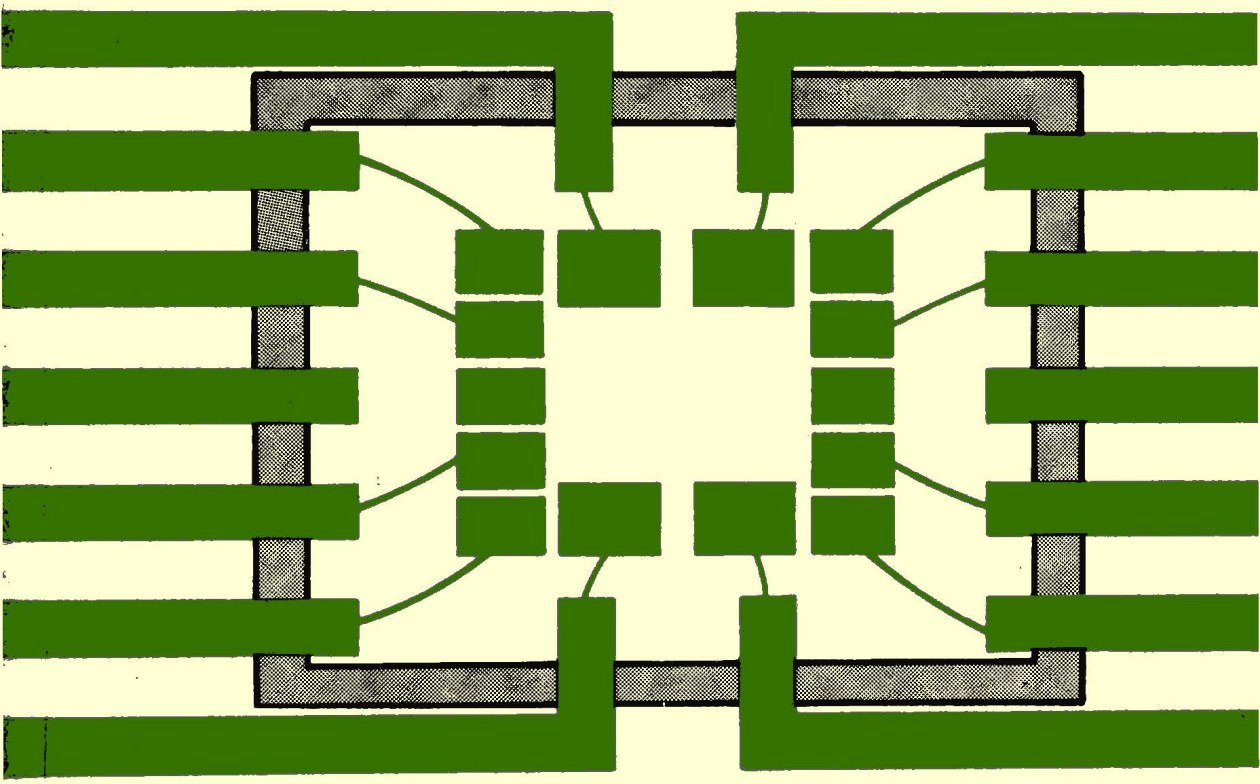
110

CMOS DIGITAL IC PROJECTS FOR THE HOME CONSTRUCTOR



R.M.Marston

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PREFACE

The most important development to have taken place in the digital integrated circuit field within the past decade has been the introduction of the technology known as COS/MOS, COSMOS, or CMOS, etc, and which is referred to simply by the RCA trade name of COS/MOS throughout this volume. COS/MOS digital ICs have considerable advantages over older digital IC types such as RTL, DTL, and TTL. In particular, they can readily be operated from unregulated supply voltages in the range 5 V to 15 V, draw virtually zero standby current, and have near-infinite input impedances. COS/MOS digital ICs have a multitude of applications in the home, in the car, and in industry.

This book is intended to be of equal interest to the electronics amateur, student and engineer. With this aim in mind, the volume starts off by outlining the basic operating characteristics of COS/MOS digital ICs, and then goes on to show 110 useful projects in which the devices can be used. All of these projects have been designed, built and fully evaluated by the author, and range from simple inverter and gate circuits to complex electronic alarm systems. Many of the projects use advanced design concepts, and are of considerable technical interest. The operating principle of each project is explained in concise but comprehensive terms, and brief constructional notes are given where necessary.

All of the projects are designed around inexpensive and readily available semiconductor devices, of American manufacture. The outlines and pin notations of all semiconductors mentioned in the volume are given in the appendix, as an aid to construction. Unless otherwise stated, all resistors used in the projects are standard half-watt types.

CHAPTER 1

AN INTRODUCTION TO COS/MOS

Digital integrated circuits have been available for a good many years now, and most readers will be familiar with common family logic names like RTL (resistor-transistor logic), DTL (diode-transistor logic), TTL (transistor-transistor logic), and ECL (emitter-coupled logic). Each of these families offers its own particular advantages when compared to the other types, but all of the families share a number of common disadvantages.

The chief disadvantages of the more common logic families are:
(1) High quiescent current requirements (typically 5 mA per gate):
(2) Tight power supply requirements (power supplies typically have to be regulated to ± 10%):
(3) Low input impedances (typically a few hundred ohms per gate):
(4) Poor noise immunity (meaning that gates can easily be triggered by spikes on the supply lines).

In the early 1970s a new and quite amazing type of digital IC appeared on the scene, and started pushing all the older families into obsolescence in low to medium-speed applications. This new family of devices is known as COS/MOS (complimentary-symmetry metal oxide silicon) digital ICs, and suffer from none of the disadvantages of the earlier families.

Typically, COS/MOS ICs draw an incredibly low quiescent current of only 0·0001 μA per gate, and can be used with unstabilised power supplies giving voltages anywhere in the range 5 V to 15 V (special versions of COS/MOS ICs can operate as low as 1·3 V). Each COS/MOS logic gate has an input impedance of about a million megohms, but is

fully protected against damage by static charges via built-in safety circuitry.

COS/MOS ICs have inherently good noise immunity, and can safely tolerate input spikes up to about 50% of the supply voltage without being upset. Finally, COS/MOS ICs have excellent thermal characteristics. Low-cost commercial types of COS/MOS ICs are designed to operate over the temperature range −40°C to + 85°C, while the more expensive military versions can operate from −55°C to + 125°C.

COS/MOS digital ICs are incredibly versatile devices, and in following chapters of this book we will look at 110 different ways of using them to make projects for use in the home, in the car, and in industry. Before going on to look at the first of these projects, however, let us take a brief look at the operating principles of COS/MOS ICs.

Understanding COS/MOS ICs

The simplest type of digital circuit that occurs in any logic family is the inverter or NOT gate. The symbol of a NOT gate is shown in *Figure 1.1a*, and its resistor-transistor equivalent is shown in *Figure 1.1b*. Operation of the circuit is quite simple. Input and output are

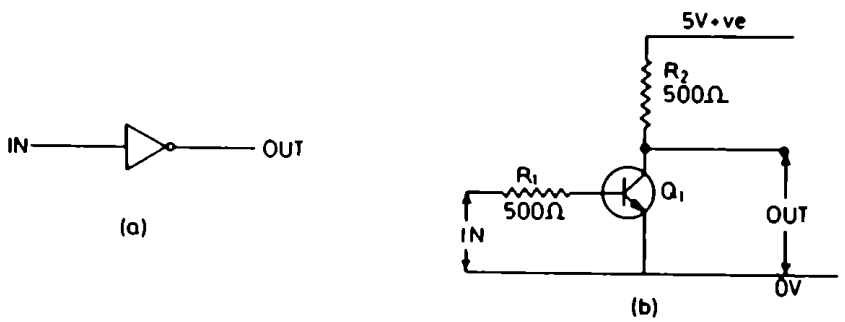


Figure 1.1 Shows (a) The symbol of a digital inverter or NOT gate, and (b) shows its resistor - transistor equivalent circuit.

always either low (grounded or at logic 0) or high (at positive supply voltage or logic 1). Suppose that the input to the circuit is at logic 0. In this case zero base drive is applied to transistor Q_1, so that the transistor is cut off and the output is at logic level 1. Note in this case that the quiescent current of the circuit is equal to the leakage current of the transistor, and is virtually zero.

Suppose now that the input to the *Figure 1.1* circuit is set to the high or logic 1 level. In this case heavy base drive is applied to Q_1 via R_1, so that the transistor is driven to saturation and the output falls to logic level 0. Note that under this condition the quiescent current of

the circuit rises to about 10 mA. Also note that the output of this simple circuit is always inverted relative to the input.

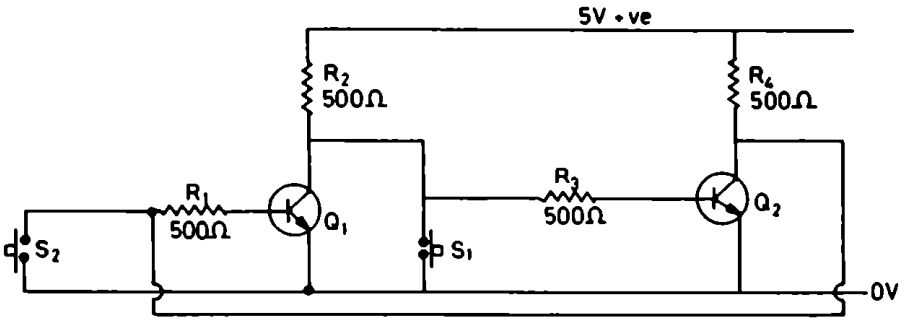


Figure 1.2 Simple manually-triggered resistor-transistor 'memory' circuit draws a quiescent current of 10 mA

A simple manually-triggered 'memory' circuit can be made up from two NOT gates by cross-coupling them as shown in *Figure 1.2.* In this case, if we press S_1 we set the input of Q_2 to logic 0, so that the output of Q_2 goes to logic 1 and drives Q_1 on and thus reduces the Q_1 output to logic 0. Because of the cross-coupling, the circuit stays locked in this state once S_1 is released, and thus the circuit acts as a simple memory. The state of the memory can be changed, if required, by momentarily closing S_2, in which case the output of Q_1 goes to logic

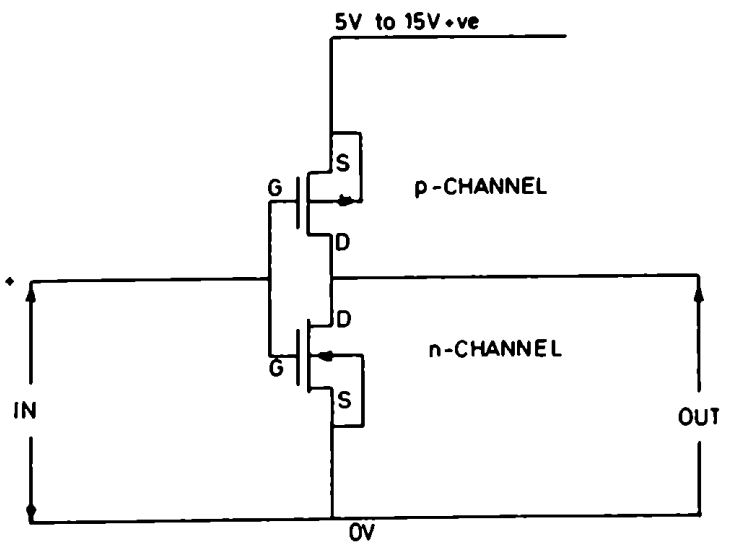


Figure 1.3 Basic COS/MOS digital inverter or NOT gate.

1 and the output of Q_2 goes to logic 0. The important point to note here is that one or other of the transistor NOT gates is switched hard on (saturated) at all times, irrespective of the state of the memory, so that the circuit draws a constant quiescent current of about 10 mA.

So much for resistor-transistor logic. Let us now go on and see what happens in its COS/MOS equivalent.

Figure 1.3 shows the basic circuit of a COS/MOS inverter or NOT gate. The circuit consists simply of one p-channel and one n-channel insulated-gate field-effect transistor (IGFET), wired in series between the two supply lines, with the IGFET gates tied together at the input terminal and with the output taken from the junction of the two devices.

Essentially, an IGFET can be regarded as a 3-terminal voltage-controlled variable resistance. The variable resistance appears between the two terminals known as the source and the drain, and the control voltage is applied between the source and the third terminal, known as the gate. The gate typically presents an impedance of about a million megohms to incoming voltages or signals; thus the IGFET can be regarded as a voltage (rather than current) controlled device.

When a very low (near-zero) voltage is applied to the IGFET gate, the drain-to-source path of the device acts like an open-circuit resistance, and typically presents an impedance in the order of thousands of megohms. Near-zero current thus flows through the device under this condition. If the gate voltage is steadily increased, a point is reached where the drain-to-source resistance just starts to fall. This point is known as the *threshold*, and threshold voltages are usually between 2V and 3V in COS/MOS IGFETs.

As the gate voltage is increased beyond the threshold, the drain-to-source resistance falls further and eventually falls to a minimum effective value of roughly 400Ω. The resistance cannot fall below this approximate value, no matter how much further the gate voltage is increased, and so a safe limit is automatically set on the maximum current that can flow through the device.

Let us go back to our *Figure 1.3* circuit, in which we are concerned mainly with input signals that are *low* (below the threshold of the n-channel IGFET but above that of the p-channel device) or *high* (above the threshold of the n-channel IGFET but below that of the p-channel device).

Suppose first that we have a logic 0 (low) input to the circuit. In this case the n-channel (lower) IGFET is cut off and is acting like a virtual open circuit resistor with an impedance of about 10 000 MΩ, but the p-channel (upper) IGFET is biased hard on and acts like an impedance of only 400Ω.

This situation is illustrated in the equivalent circuit of *Figure 1.4a*, where it can be seen that the two IGFETs act like a resistive potential divider in which the output is high (at logic 1) and is essentially strapped to the positive supply line via the 400Ω resistance, and in which

the quiescent current of the divider is limited to the nanoamp region by the high value of the 10 000MΩ resistor.

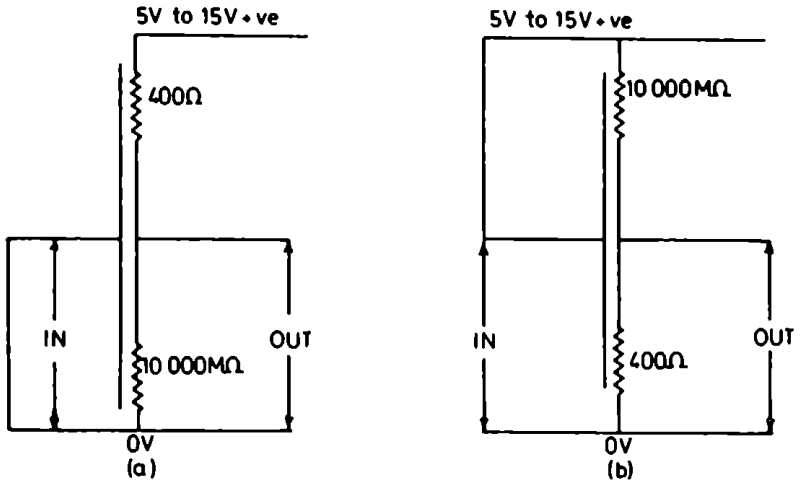


Figure 1.4 Equivalent circuit of COS/MOS NOT gate with (a) logic O input, and (b) logic 1 input.

Suppose now that the input voltage is slowly increased in a positive direction. The device current is virtually zero until the input voltage exceeds the threshold of the n-channel IGFET, at which point the effective resistance of the n-channel device starts to decrease and that of the p-channel IGFET starts to increase. Under this condition the device current is dictated by the larger of the two resistances, and is of measurable proportions. When the input voltage is appreciably *less* than half of the supply volts the resistance of the n-channel IGFET is much greater than that of the p-channel device, and thus the output of the circuit is high or at logic level 1. When the input voltage is appreciably *more* than half of the supply volts the resistance of the n-channel IGFET is much less than that of the p-channel device, and thus the output of the circuit is low or at logic level 0.

When the input voltage is at approximately half-supply volts, a point is reached where both IGFETs attain roughly the same value, and at this point the device starts to act like a linear amplifier, and a current of several milliamps may flow through the circuit. In practice, a semi-regenerative switching action usually takes place at this point, and the output swings sharply from one logic state to the other.

The value of input voltage needed to initiate this switching action is known as the *transition* voltage, and is usually specified as a percentage of the supply voltage. Transition voltages vary between 30% and 70% of the supply voltage in practical COS/MOS devices.

Finally, consider the case where the input to the *Figure 1.3* circuits is high or at logic 1. In this case the p-channel IGFET is cut off and

acting like a virtual open circuit, while the n-channel IGFET is biased hard on and is acting like a 400Ω resistor. This situation is shown in *Figure 1.4b*, where it can be seen that the two IGFETs again act like a potential divider, but in this case the 400Ω resistor is at the low end, so the output is low (at logic 0) and is essentially strapped to ground via 400Ω. The quiescent current of the network is again limited to the nanoamp region by the larger of the two resistors.

Thus, the *Figure 1.3* circuit acts as a conventional digital inverter or NOT gate, but has the following unique properties.

(1) *An exceptionally high input impedance* (about a million megohms).

(2) *It draws negligible quiescent current* from the supplies (about 1 nA), irrespective of its logic state.

(3) *It can be operated from a wide range of supply voltages* (typically 5V to 15V), since its minimum voltage requirement is limited only by the threshold characteristics of its IGFETs, and the maximum is limited only by the breakdown characteristics of the devices.

(4) *Its output can swing from zero to the full positive supply rail voltage*, since no potentials are lost in the circuit via saturation voltages or forward biased junction voltages.

(5) *The device cannot be damaged by shorts at its output*, since the maximum current of the device is limited by the 400Ω minimum impedance of the ON IGFET.

Figure 1.5 shows how two COS/MOS NOT gates can be cross-coupled to form a simple manually-triggered memory circuit. This

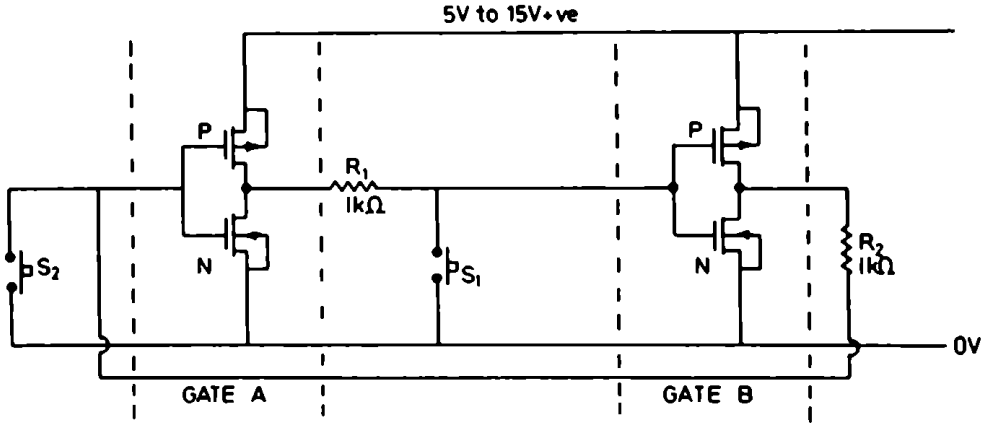


Figure 1.5 Manually-triggered COS/MOS 'memory' circuit draws a quiescent current of 0·002 μA

circuit operates in a similar way to that of *Figure 1.2*. When S_1 is momentarily closed the input to gate B is set at logic 0, so that the

output of gate B goes to logic 1 and in turn drives the output of gate A to logic 0.

The circuit remains in this state when S_1 is released, due to the cross-coupling between the two gates; thus the circuit acts as a simple memory. The state of the memory can be changed by momentarily closing S_2, in which case the output of gate A goes to logic 1, and the output of gate B goes to logic 0.

The most important practical difference between the resistor-transistor memory circuit of *Figure 1.2* and the COS/MOS circuit of *Figure 1.5* is that the resistor-transistor circuit draws a quiescent current of 10 mA, while the COS/MOS version draws a quiescent current of only 0.002μA. Thus, the resistor-transistor version draws five million times more quiescent current than its COS/MOS equivalent.

The reader may at this stage be thinking that this notion of a logic circuit drawing virtually zero supply current sounds too good to be true, and that there must be a catch in this COS/MOS business somewhere. The simple answer is that a COS/MOS circuit does in fact draw a significant current, but only as it is going through the actual motion of changing logic states, and not when it is in the quiescent condition.

Each time COS/MOS changes state, it draws a pulse of current from the supply. The more often it changes state in a given time, the greater are the number of current pulses that it takes from the supply and the greater is the *mean* current that it consumes. Thus, the mean current that it takes is directly proportional to the frequency of its operation.

At frequencies of 5 MHz, COS/MOS logic draws roughly the same current as its TTL equivalent. At 5 kHz, it draws only one thousandth of the current of TTL. Consequently, COS/MOS is best suited to low or medium-speed applications, although it is capable of operating as high as 10 MHz when needed.

Having cleared up these basic points, let us go on and look at two practical COS/MOS digital ICs.

The CD4001 and the CD4011

Several manufacturers produce ranges of COS/MOS digital ICs. Leaders in the field are RCA, and one of the most useful and versatile ICs in their range is a quad 2-input NOR gate which is known as the CD4001. Motorola produces an identical device under the coding of MC14001.

Figure 1.6 shows the logic circuit and pin connections of the CD4001 IC which is encapsulated in a 14-pin dual-in-line plastic or ceramic package. As you can see, two of the pins are used for supply

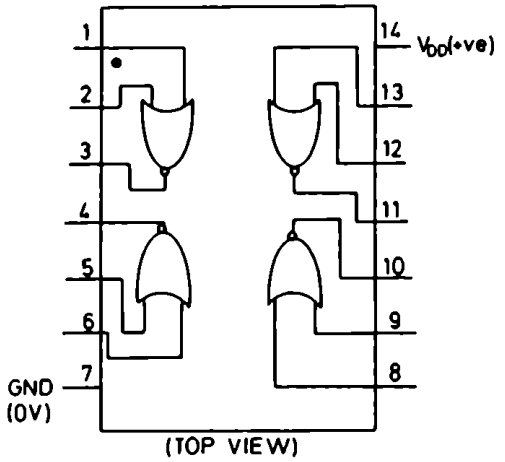


Figure 1.6 Logic diagram and pin connections of the CD4001 quad 2-input NOR gate.

connections (pin 7 goes to ground and pin 14 goes to the positive supply line), and the rest of the pins connect to the input or output terminals of the NOR logic gates. There are four identical 2-input NOR logic gates in each IC package.

Figure 1.7 shows the actual circuit that is used in each of the 2-input NOR gates. Here, two series-connected p-channel IGFETs are wired in

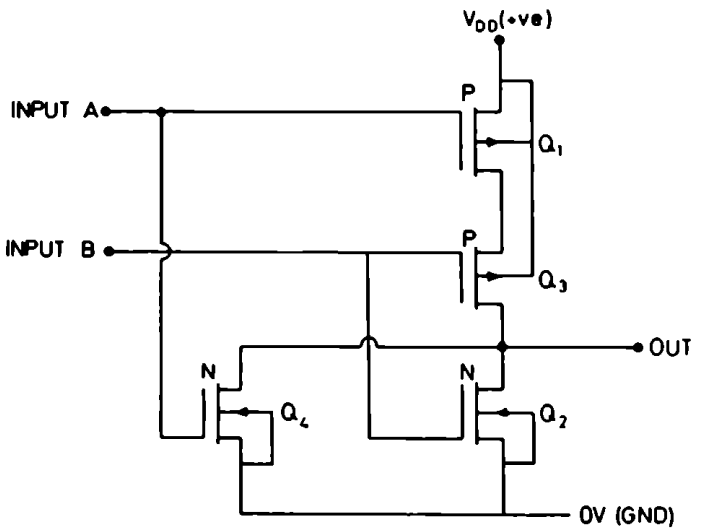


Figure 1.7 Circuit of each of the four 2-input gates of the CD4001.

series with two parallel-connected n-channel IGFETs. Each of the two input terminals is connected to the gates of one of the p- and n-channel IGFET pairs. Circuit operation is as follows.

Suppose first that both input terminals are grounded or at logic level 0. In this case both of the n-channel IGFETs are biased below their threshold points and act like open-circuit resistors, and both of the p-channel IGFETs are biased hard on and act like 400Ω resistors. The output of the circuit is thus high and at logic level 1 under this condition. The output is thus inverted relative to the inputs.

Suppose now that input A is at logic level 1 and that input B is at logic 0. In this case Q_2 acts like an open-circuit resistor and Q_3 acts like 400Ω, due to the 0 input on terminal B, but Q_1 acts like an open-circuit resistor and Q_4 acts like 400Ω, due to the 1 input on terminal A. Since Q_1 is in series with Q_3, and Q_2 is in parallel with Q_4, the result is that the top half of the circuit acts like an open circuit and the lower half acts like 400Ω. Consequently, the output of the circuit is low and at logic 0 under this condition.

Suppose next that input A is at logic level 0 and input B is at logic 1. This situation is similar to that outlined above, except that in this case Q_3 and Q_4 act like open circuits, and Q_1 and Q_2 act like 400Ω resistors. The net result is the same however, and the top half of the circuit acts like an open circuit and the lower half acts like 400Ω, so that the output of the circuits is again at logic 0 under this condition.

Finally, suppose that both inputs are at logic level 1. In this case both of the upper IGFETs act like open circuits and both of the lower IGFETs act like 400Ω resistors, so that the output is again low at logic 0.

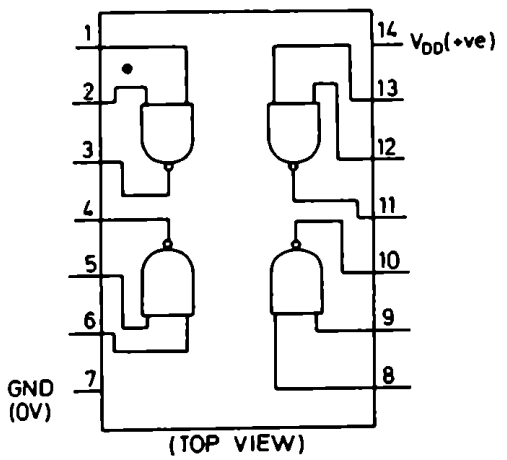


Figure 1.8 Logic diagram and pin connections of the CD4011 quad 2-input NAND gate.

Thus, the output of the NOR gate goes to logic 1 only when both inputs are at logic 0, and goes to logic 0 when either input is at logic 1. Note that the circuit can be made to function as a simple inverter or NOT gate by shorting inputs A and B together.

Another useful member of the RCA COS/MOS family of digital ICs is the quad 2-input NAND gate known as the CD4011. *Figure 1.8* shows the logic circuit and pin connections of this device, and *Figure 1.9* shows the actual circuit that is used in each of its four 2-input NAND gates. The action of each gate is such that its output goes to logic 0 only when both inputs are at logic 1, and goes to logic 1 if either input is at logic 0.

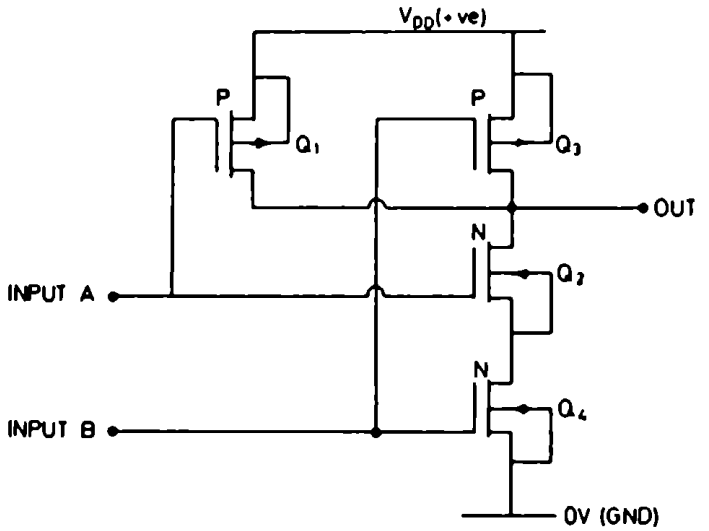


Figure 1.9 Circuit of each of the four 2-input gates of the CD4011

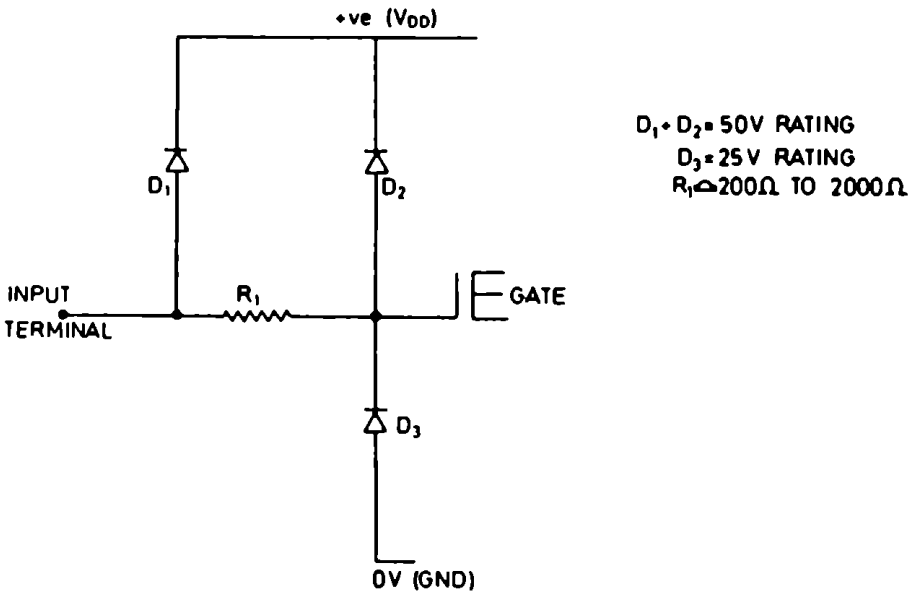


Figure 1.10 COS/MOS gate input protection circuit that is connected to each of the eight input terminals of the CD4001 and CD4011.

All input terminals of the CD4001 NOR gate and the CD4011 NAND gate IC (and all other digital ICs in the COS/MOS family) have

input impedances of about a million megohms, but are fully protected against damage from static charges via the input safety circuit shown in *Figure 1.10.* Each of the eight input terminals of the CD4001 and CD4011 are protected by one of these diode-resistor safety circuits.

The CD4001 and CD4011, like all COS/MOS digital ICs, are extremely rugged devices and can withstand considerable abuse without suffering permanent damage. Their outputs, for example, are fully short-circuit proof. There are in fact only three ways in which you can damage a COS/MOS circuit, and one of these is to connect the supply lines in the wrong polarity, in which case heavy current will flow through the D_2 and D_3 protection diodes and damage the substrate.

One other way you can damage a COS/MOS IC is to connect a very low impedance input signal to it when its power supplies are switched off, and the remaining way is to connect the device to a very low impedance input signal that has such a large amplitude that it goes above the positive supply line voltage. In either case, a heavy current will flow through protection diode D_1 and the substrate will again be damaged. Both of these potential sources of damage can be eliminated by simply wiring a 1000Ω resistor in series with each input terminal so that any current that does flow is limited to a safe value of a few milliamps.

Using COS/MOS

COS/MOS digital ICs are very easy devices to use, provided you obey the following basic rules.

(1) Always make sure that power lines are in the correct polarity before you apply power to the IC.

(2) Never connect very low impedance energy sources (including storage capacitors) directly to the device input terminals; always connect them via a 1000Ω or greater current-limiting resistor.

(3) Always tie unused input terminals directly to ground or to the positive supply line, depending on the logic requirements.

(4) Never let used input terminals float; always take them to ground or to the positive line via a high value resistance.

When you buy your first RCA COS/MOS IC, you'll find that it has a one or two-letter suffix added at the end of its basic code number. This suffix relates to the style of packaging of the device and to its voltage and temperature operating ranges. Details of the meanings of the five available suffix codes are shown in *Table 1.1.* Thus, the CD4001AD is a quad 2-input NOR gate housed in a ceramic dual-in-line package and

can operate over the supply range 3V to 15V and the temperature range −55°C to + 125°C, while the CD4001E is in a plastic dual-in-line package and can only operate over the supply range 5V to 15V and the temperature range −40°C to +85°C.

Table 1.1. Meanings of suffix codings of RCA COS/MOS ICs

Suffix Coding	*Package*	*Operating voltage range*	*Operating temperature range*
AD	Ceramic d.i.l.	3 V to 15 V	-55 °C to + 125 °C.
AE	Plastic d.i.l.	3 V to 15 V	-40 °C to + 85 °C.
AK	Flat pack	3 V to 15 V	-55 °C to + 125 °C.
D	Ceramic d.i.l.	5 V to 15 V	-55 °C to + 125 °C.
E	Plastic d.i.l.	5 V to 15 V	-40 °C to + 85 °C.

Most of the 110 practical COS/MOS IC projects described in the remaining chapters of this book are designed to operate with supply voltages in the range 5 V to 15 V and can be used with any of the specified types of ICs, irrespective of their suffix codings. In most cases, however, the circuits can be made to operate with supply voltages as low as 3V by simply using them with ICs that have suffix numbers AD, AE, or AK.

Having cleared up these basic points, let us now go on and look at some practical COS/MOS IC applications.

CHAPTER 2

15 INVERTER, GATE, AND LOGIC CIRCUITS

CD4001 quad 2-input NOR gate and CD4011 quad 2-input NAND gate ICs can readily be used in a variety of pulse inverting and gating applications, and can be made to perform all of the five basic logic functions used in digital circuitry. The near-infinite input impedances, near-zero standby currents, and wide supply rail tolerances of these COS/MOS ICs make them particularly suitable for use in these applications, and a range of practical circuits of these types is shown in this chapter.

Inverter circuits

A pulse inverter or sign changer is the simplest type of element that is used in digital circuitry, and is given the symbol shown in *Figure 2.1a.* The circuit gives a high or 'logic 1' output when its input is low or at 'logic 0', and gives a low output when its input is high.

An inverter can be made up from a NOR gate or a NAND gate by simply shorting both of the gates input terminals together, as shown in *Figures 2.1b* and *2.1c.* Note in these two circuits that, since only one of the four available gates of each IC is used in this application, the input terminals of the remaining three unused gates are taken directly to ground.

All four gates can be used as pulse inverters, if required, by using the connections shown in the quad pulse amplifier/inverter circuit of *Figure 2.1d.*

A slightly more complex circuit is the non-inverting pulse amplifier or buffer, which uses the symbol shown in *Figure 2.2a.* A circuit of this

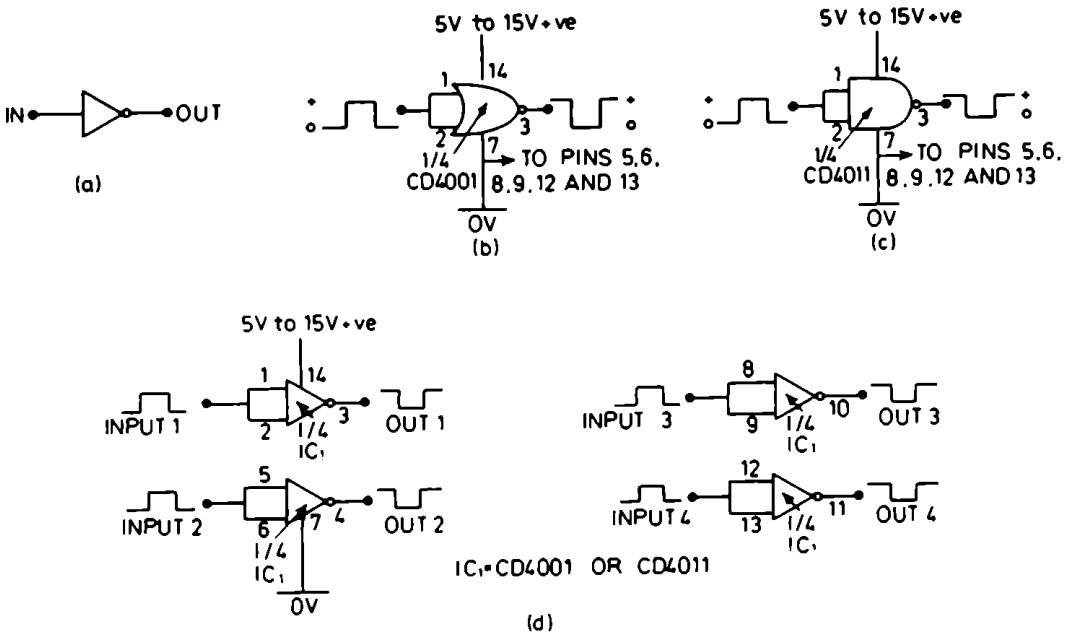


Figure 2.1a Basic inverter symbol; b Simple pulse amplifier/inverter; c Alternative pulse amplifier/inverter; d Quad pulse amplifier/inverter

type can be made by simply wiring two inverters in series, and *Figure 2.2b* shows how two of the gates of a CD4001 can be used for this application: a similar circuit can be made from a CD4011 IC. Note that

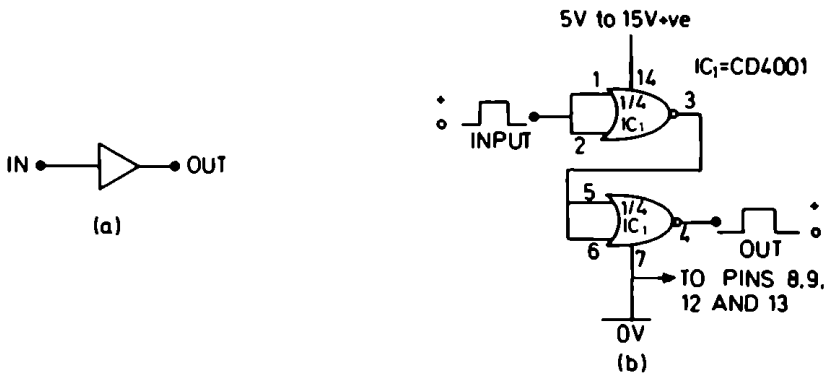


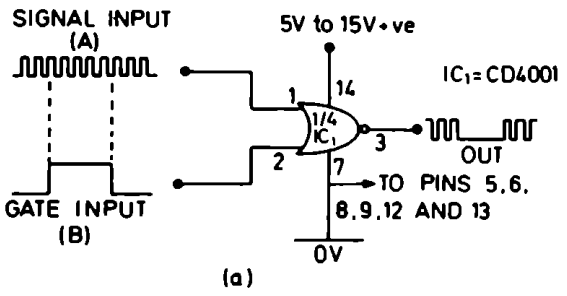
Figure 2.2a Symbol of non-inverting pulse amplifier or buffer; b Practical non-inverting pulse amplifier circuit

two of these non-inverting amplifiers can be made from each CD4001 or CD4011 package.

Gate circuits

Pulse gates can be simply described as pulse inverters or buffers that can be 'enabled' and 'disabled', or turned on and off, via an electronic signal, on command. One of the simplest circuits of this type is the pulse disabling gate, and *Figure 2.3a* shows how a CD4001 IC can be used to make a gate of this type.

Here, an input signal is applied to pin 1 of the IC, and a gating or command signal is applied to pin 2. The output of the circuit is taken from pin 3. Normally, with a zero or logic 0 gating input applied, the circuit acts as a simple pulse amplifier, and produces an inverted version of the input signal at output pin 3. When, however, a logic 1 gate input



(a)

INPUT		OUT
A	B	
0	0	1
1	0	0
0	1	0
1	1	0

(b)

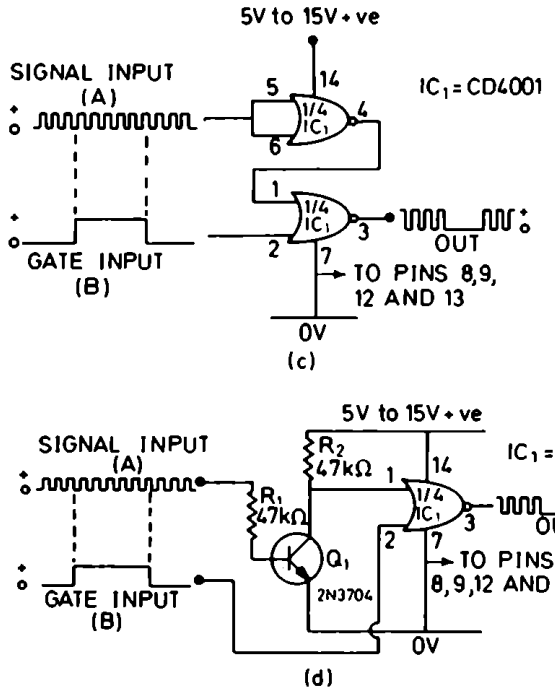
Figure 2.3a Simple pulse disabling gate; b Truth table for Figure 2.3a;

is applied to pin 2, the circuit's output is driven into the logic 0 state, and the input signal no longer appears at the output. The gate is thus 'disabled'.

Note in the *Figure 2.3a* circuit that only one of the four available CD4001 gates is used, and that all input terminals of the remaining three unused gates are taken to ground.

A further point to note about the *Figure 2.3a* circuit is that its output goes high if its input signal is removed or set to logic 0 when the circuit is enabled. This point is evident from the *truth table* of *Figure 2.3b*, which shows the four possible states of the circuit. If required, the circuit can be made to give an output that is low under the above condition by simply interposing an inverter stage between the input signal and the input of the gate. This inverter can be made from a spare gate of the CD4001 IC, as in the modified pulse disabling gate circuit of *Figure 2.3c*, or it can be a simple direct-coupled transistor amplifier, as in the alternative modified pulse disabling gate circuit of *Figure 2.3d*. *Figure 2.3e* shows the truth table for the circuits of *Figures 2.3c* and *2.3d*.

An advantage of the transistor version of the pulse disabling gate shown in *Figure 2.3d* is that the circuit can be activated by any input signal pulses that vary alternately from less than 200 mV to greater that 1 V. In the *Figure 2.3c* circuit these pulses have to fluctuate fully between the logic 0 and logic 1 levels.

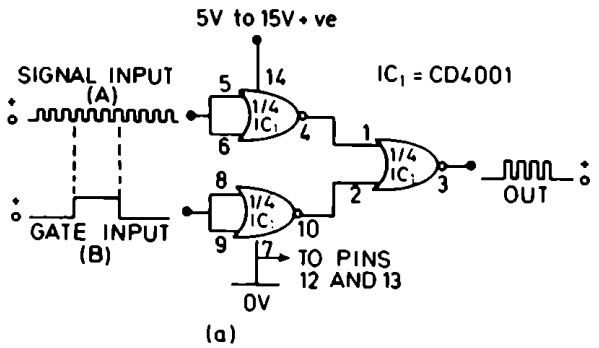


INPUT		OUT
A	B	
0	0	0
1	0	1
0	1	0
1	1	0

(e)

Figure 2.3c Modified pulse disabling gate; d Alternative modified pulse disabling gate; e Truth table for Figures 2.3c and 2.3d

A pulse disabling gate can readily be converted into a pulse enabling gate, which passes signals only when the gating input is high or at logic level 1, by simply interposing an inverter stage between the gating input



INPUT		OUT
A	B	
0	0	0
1	0	0
0	1	0
1	1	1

(b)

Figure 2.4a Pulse enabling gate; b Truth table for Figure 2.4a

signal and the gate input pin of the disabling gate. *Figure 2.4a* shows how the *Figure 2.3c* circuit can be converted into a pulse enabling gate. *Figure 2.4b* shows the truth table of the circuit.

The pulse enabling gate of *Figure 2.4a* can be converted to an electronically- or manually-triggered START/STOP gate, which starts passing signals at a START command and stops passing them on a

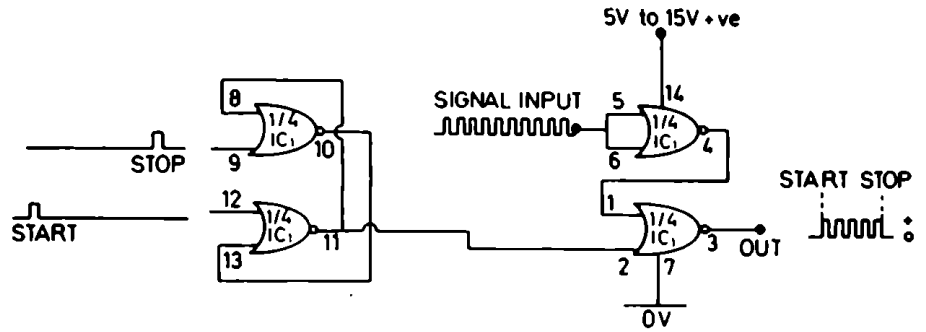


Figure 2.5 Electronically-triggered START/STOP gate

separate STOP command, by feeding the command signals to the gate via a simple bistable multivibrator element. *Figure 2.5* shows the electronically-triggered version of such a circuit, and *Figure 2.6* shows the manually-triggered version.

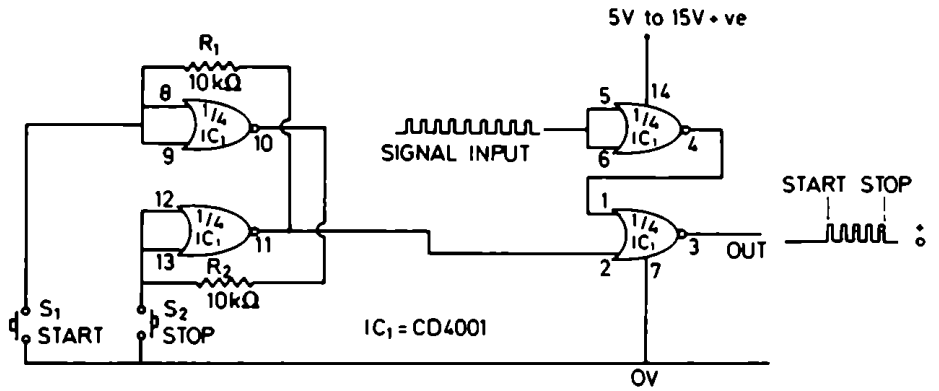


Figure 2.6 Manually-triggered START/STOP gate

The two circuits operate in the same basic way, and use the two left-hand CD4001 gates as a bistable multivibrator, and use the two right-hand gates as actual gating elements. Normally, the output of the bistable is high or at logic 1, so that the gating circuit's output is grounded, and none of the input signal reaches the output terminal. When the START command is given the bistable changes state, and locks into this new state even when the command signal is subsequently removed. As the bistable changes state its output goes to logic level 0, and the gate opens and passes the input signals to its output. These signals continue to flow unitl a STOP command is given, at which point the bistable flips back to its original 'logic 1' condition, and the gate closes again and the input signal stops reaching the output.

A practical application of the START/STOP gate is in a sports-event timer. In this application the signal input is derived from an accurate 1 kHz crystal-controlled oscillator, and the gates output is taken to an electronic counter. The START command signal can be derived from the race-starter's gun, and the STOP signal can be derived from the photocell of a light beam unit projected across the finishing line.

As soon as the starter's gun is fired the gate opens and starts feeding 1 kHz pulses to the counter. As soon as the winner reaches the finishing line and breaks the light beam the gate closes, and the 1 kHz pulses stop reaching the counter. Thus, the number of pulses registered on the counter from the 1 kHz oscillator are equal to the duration of the race, to the nearest millisecond. For longer races the oscillator can be a 1 Hz type, in which case the counter will register the race time in seconds.

A variation of the START/STOP gate is the bistable gate. This circuit uses only a single trigger-input terminal, and the circuit action is such that the gate alternately opens and closes on successive input trigger pulses. Thus, the gate may open the first time that a trigger pulse is applied, and will then remain open until a second trigger pulse arrives, at which point the gate will close again. The gate will then remain closed until a third pulse arrives, at which point the gate opens again, and so on *ad infinitum*. *Figure 2.7* shows the practical circuit of an electronically-triggered bistable gate, and *Figure 2.8* shows a manually-triggered version of the same circuit.

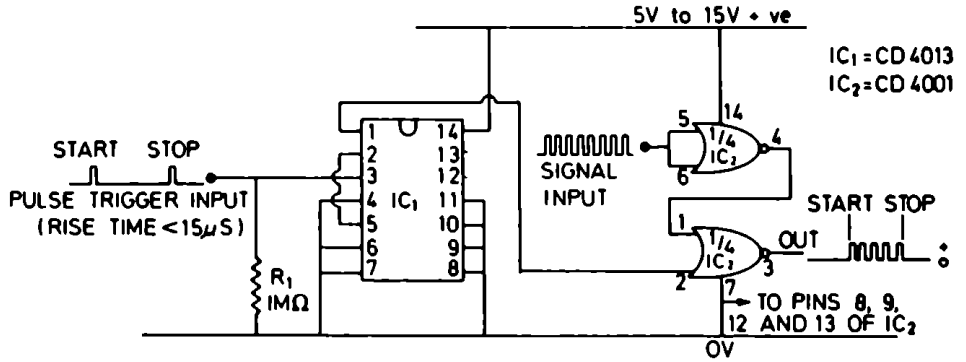


Figure 2.7 Electronically-triggered bistable gate

The operation of the *Figure 2.7* circuit is quite simple. The CD4013 is a dual 'D'-type flip-flop or divide-by-two IC. With the connections shown, only one of these flip-flops is used, and its action is such that its output, taken from pin 1, switches alternately between the low (logic 0) and high (logic 1) states when successive trigger pulses are applied to input pin 3. These trigger pulses must themselves be so shaped that they have rise times of less than 15 μS, and their amplitudes must switch fully between the logic 0 and logic 1 levels.

Assume, then, that the output of the CD4013 is in the high state. Under this condition the gate formed by the CD4001 IC is disabled and its output is locked into the low state, so that no part of the input signal

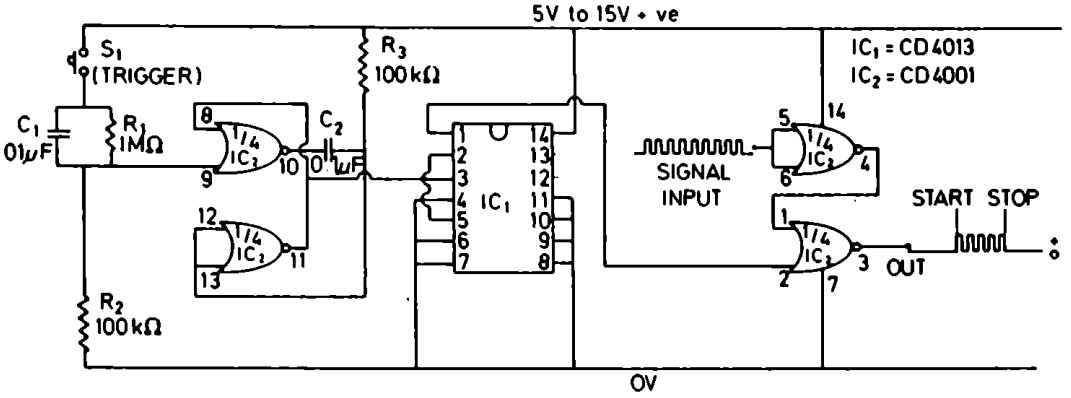


Figure 2.8 Manually-triggered bistable gate

reaches the output at pin 3. When a trigger pulse is applied to the input of the CD4013 the bistable changes state, and in doing so it enables the gate circuit and allows the input signals to reach the output at pin 3. The gate remains enabled until a second trigger pulse is applied to the CD4013, at which point the bistable changes back to its original state, and the gate turns off again. The sequence then repeats *ad infinitum*.

The manually-triggered version of the bistable gate is similar to that described above, except that the trigger pulse to the CD4013 bistable element is derived from push-button switch S_1 via a simple monostable or one-shot multivibrator formed from two of the gates of the CD4001.

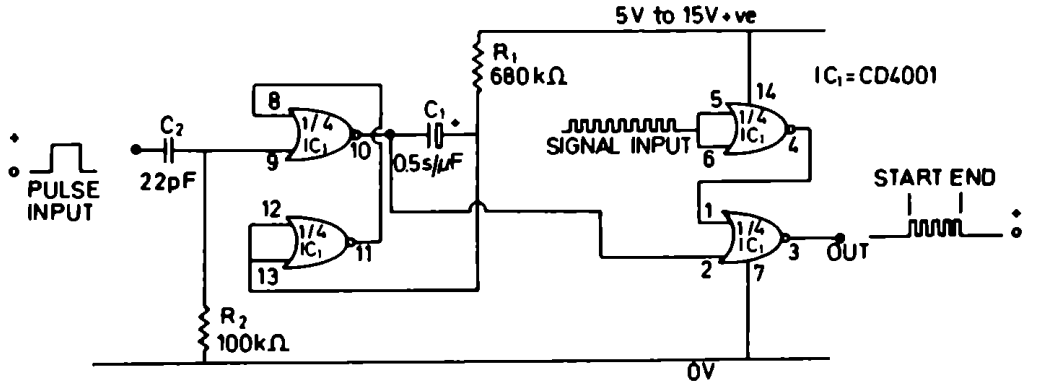


Figure 2.9 Electronically-triggered one-shot gate

Each time S_1 is pressed the monostable generates a brief fast rise-time pulse, which causes the CD4013 to change states and thus enable or disable the gate circuit. The circuit actually changes state at the moment that the contacts of S_1 close, and the circuit action is unaffected by the duration of the actual switch closure.

Finally, another type of gate is the one-shot or auto-turn-off type, which is normally closed, but which opens as soon as an input trigger pulse is applied and then turns off again automatically after a pre-set period. *Figure 2.9* shows the electronically-triggered version of such a circuit, and *Figure 2.10* shows the manually-triggered version.

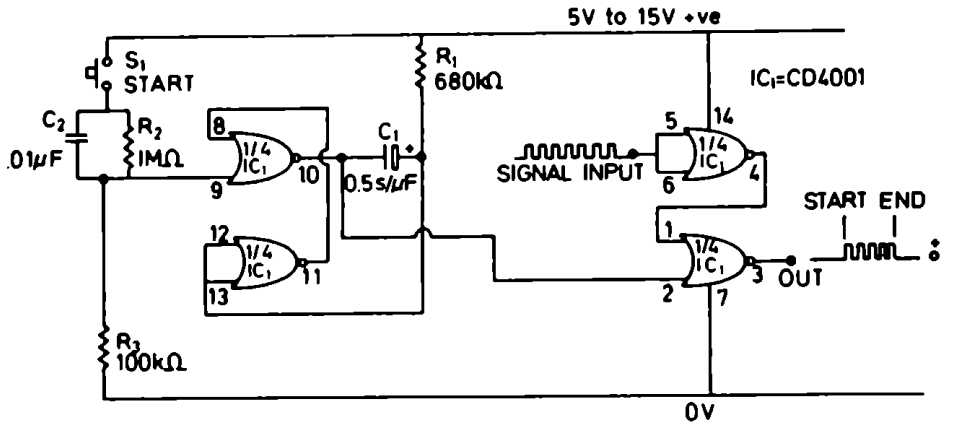


Figure 2.10 Manually-triggered one-shot gate

The two circuits operate in the same basic way. Two of the gates of the CD4001 IC are used to make a monostable multivibrator. The output of this monostable, taken from pin 10 of the IC is normally high or at logic 1; thus the gate is disabled and the input signals fail to reach the pin 3 output of the circuit. When a trigger pulse is applied to pin 9 of the IC the monostable fires and its output goes low, thus enabling the gate and allowing the input signals to reach output pin 3. After a pre-set delay (determined by C_1 and R_1) the monostable automatically turns off again and its output returns to the logic 1 state, so that the gate becomes disabled and the input signals stop reaching output pin 3.

In the electronically-triggered *Figure 2.9* version of the circuit the monostable is triggered by applying a pulse or square-wave signal to pin 9 of the IC via C_2. C_2 works with R_2 and the built-in protection diodes of the IC to differentiate this input waveform in such a way that the trigger waveform actually reaching pin 9 is independent of the duration of the original input signal. The only requirement of this input signal is that it must have a rise time of less than 2μS.

In the manually-triggered *Figure 2.10* version of the circuit the monostable is triggered by a pulse derived from the positive supply line by the action of closing push-button START switch S_1. The gate actually opens at the moment that the contacts of S_1 close, and the duration of the gate opening is unaffected by the duration of the actual switch closure.

The monostable period of the circuits of *Figures 2.9* and *2.10* is determined by the time-constants of C_1 and R_1. When R_1 is given the value shown, the period works out at approximately 0.5 s/μF of C_1 value. Periods can be varied from a fraction of a millisecond to tens of seconds by chosing a suitable C_1 value. The period can be made variable, if required, by using a variable resistor in place of R_1.

Logic circuits

CD4001 and CD4011 COS/MOS ICs can be used to perform all five of the basic functions used in logic circuitry.

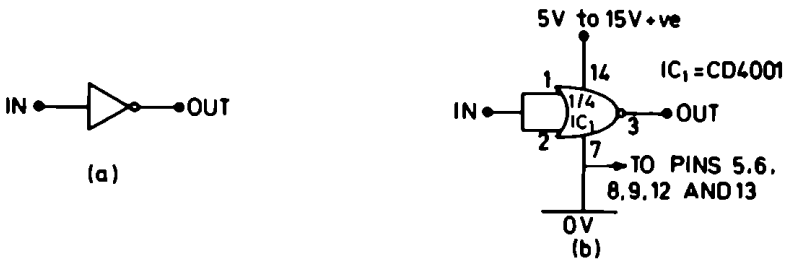


Figure 2.11a NOT logic symbol; b NOT logic circuit

The most basic of all logic elements is the NOT logic circuit, which uses the symbol shown in *Figure 2.11a.* This circuit is simply a pulse inverter, and gives a high output when a low or zero input is applied, and gives a low output when a high input is applied. *Figure 2.11b* shows how one of the gates of a CD4001 can be connected as a NOT logic element. A similar element can be made from one of the gates of a CD4011 IC, and four such elements can be built from each IC package.

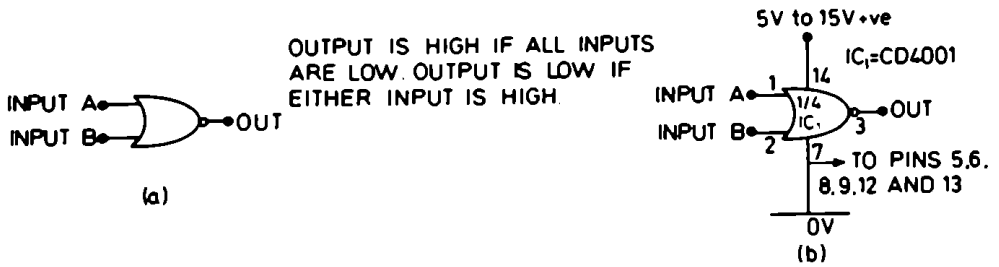


Figure 2.12a NOR logic symbol; b NOR logic circuit

Figure 2.12a shows the symbol that is used to represent a NOR logic element, and *Figure 2.12b* shows the connections for making one of these elements from one of the gates of a CD4001 IC. Four such elements can be built from each CD4001 package. The action of the

NOR logic circuit is such that its output goes high or to logic 1 only when both inputs are low or at logic 0: the output goes low if either input is high.

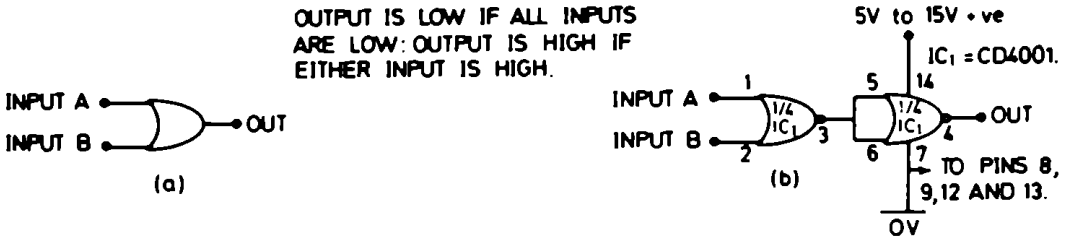


Figure 2.13a OR logic symbol; b OR logic circuit

Figure 2.13a shows the symbol that is used to represent an OR logic element, and *Figure 2.13b* shows how one of these elements can be constructed from a pair of gates from a CD4001 IC. Two such elements can be built from each CD4001 package. The action of the OR logic circuit is such that its output goes low only when both inputs are low: the output goes high if either input is high. As can be seen from *Figure 2.13b*, an OR element can be made by wiring a simple inverter in series with the output of a NOR logic circuit.

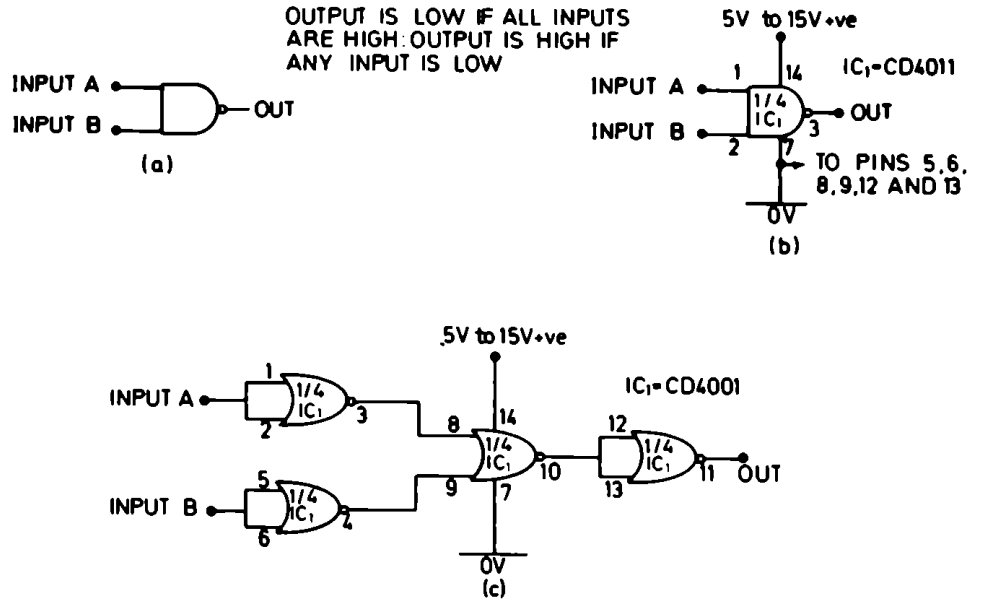


Figure 2.14a NAND logic symbol; b NAND logic circuit; c Alternative NAND logic circuit

Figure 2.14a shows the symbol that is used to represent a NAND logic element, and *Figure 2.14b* shows the connections for making one of these elements from one of the gates of a CD4011 IC. Four such elements can be built from each CD4011 package. Alternatively, *Figure 2.14c* shows how a single NAND logic circuit can be built using all four

of the gates from a CD4001 IC. The action of the NAND logic circuit is such that its output goes low only when both inputs are high: the output goes high if either input is low.

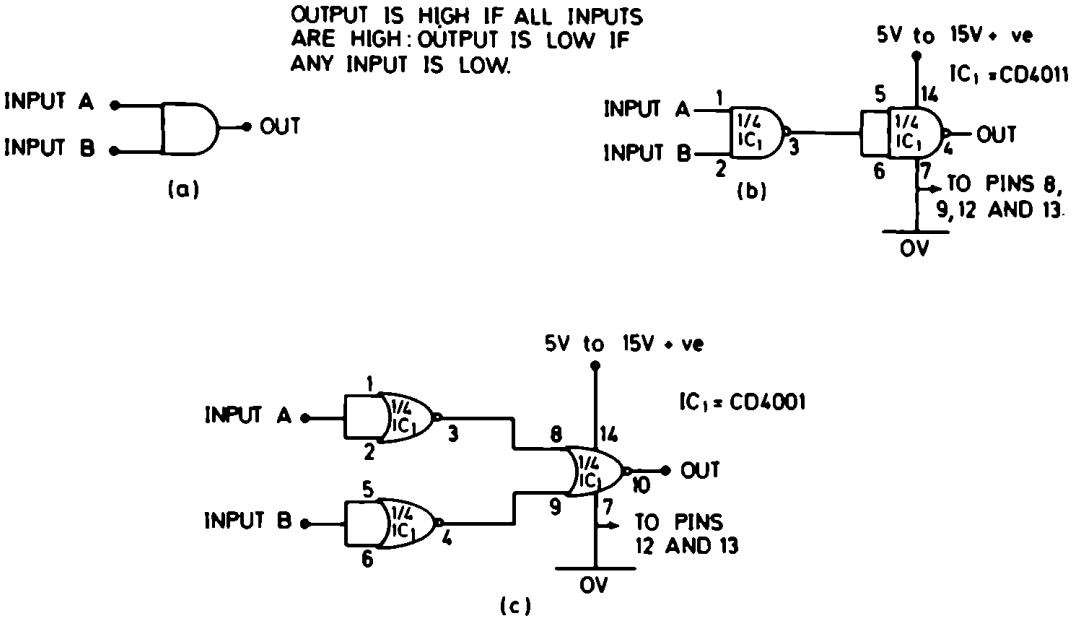


Figure 2.15a AND logic symbol; b AND logic circuit; c Alternative AND logic circuit

Finally, *Figure 2.15a* shows the symbol that is used to represent an AND logic element, and *Figure 2.15b* shows the connections for making one of these elements from a pair of CD4011 gates. Alternatively, *Figure 2.15c* shows how a single AND logic circuit can be built using three of the gates of a CD4001 IC. The action of the AND logic circuit is such that its output goes high only when both inputs are high: the output is low if either input is low.

CHAPTER 3

25 MULTIVIBRATOR CIRCUITS

The near-zero quiescent current, near-infinite input impedance, wide supply voltage tolerance, and excellent thermal stability of COS/MOS digital ICs makes them particularly suitable for use in multivibrator circuits. The ubiquitous CD4001 quad 2-input NOR gate can readily be made to function in a number of high-performance monostable and astable applications, and in a number of simple bistable or memory circuits. More advanced counting and dividing bistable circuits can be built using a variety of more specialised COS/MOS digital ICs, as shown later in this volume.

The present chapter shows 25 ways of using COS/MOS digital ICs in bistable, monostable, and astable circuits. Most of these circuits are designed around the CD4001 quad 2-input NOR gate IC.

Bistable multivibrator circuits

A simple bistable multivibrator or memory circuit can be made by cross-coupling the inputs and outputs of a pair of NOT or NOR logic gates. *Figure 3.1* shows the practical connections for making an electronically-triggered circuit of this type from two NOR gates of a CD4001.

Here, the output of gate A is direct-coupled to one of the input terminals of gate B, and the output of gate B is direct-coupled to one of the input terminals of gate A. The 'spare' input terminal of each gate accommodates an input command signal, and both are normally low or at logic level 0.

To understand the circuit operation, assume initially that the output of the circuit, taken from the output terminal of gate A, is at the low or logic 0 level. In this case both inputs of gate B are also at logic level 0, and so the output of gate B is at logic level 1. Since the output of gate B is direct-coupled to one of the input terminals of gate A, the output of gate A is driven to logic level 0. The output of gate A is thus locked in the logic 0 state by the cross-coupling under this condition.

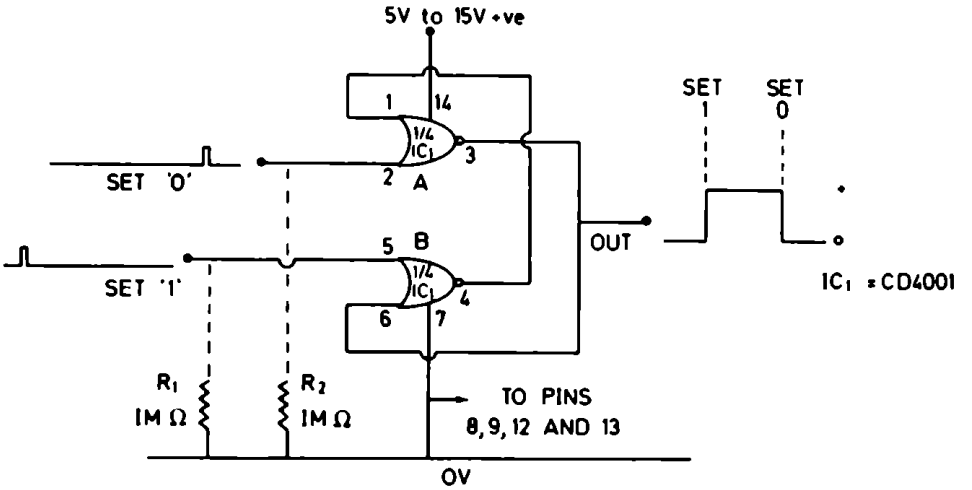


Figure 3.1 Electronically-triggered bistable multi or memory unit.

Suppose now that a positive trigger pulse is applied to the set '1' input terminal of the circuit. In this case the output of gate B drops to logic 0 for the duration of the pulse, and under this condition both input terminals of gate A are held at logic level 0, so that its output goes to logic 1. Since the output of gate A is direct-coupled to one input terminal of gate B, the output of gate B is locked in the logic 0 condition. Consequently, the output of the circuit goes to logic 1 as soon as the input set '1' pulse is applied, and the circuit then locks into this condition and stays there even when the input pulse ceases to be applied.

Finally, suppose that a positive trigger pulse is now applied to the set '0' input terminal of the circuit. In this case the output of gate A drops to logic 0 for the duration of the pulse, and under this condition both input terminals of gate B are held at logic level 0, so that the output of gate B goes to logic level 1. Since the output of gate B is direct-coupled to the input terminal of gate A, the circuit is then locked into this condition, and its output remains at the logic 0 level.

Thus, the output of the *Figure 3.1* circuit can be locked at the logic 0 or logic 1 level by applying a brief command pulse to one or other of the two input terminals. Note that these command signals should be direct-coupled from sources that switch between the logic 0 and logic 1 levels. If the command signals are to be derived from 'floating' sources,

the pin 2 and pin 5 input terminals of the bistable must be taken to ground via high-value resistors, as shown dotted by R_1 and R_2 in the diagram. Also note that two complete bistable multivibrator or memory circuits can be built from each CD4001 IC, and that each circuit draws a typical quiescent current of only 0.002 μA.

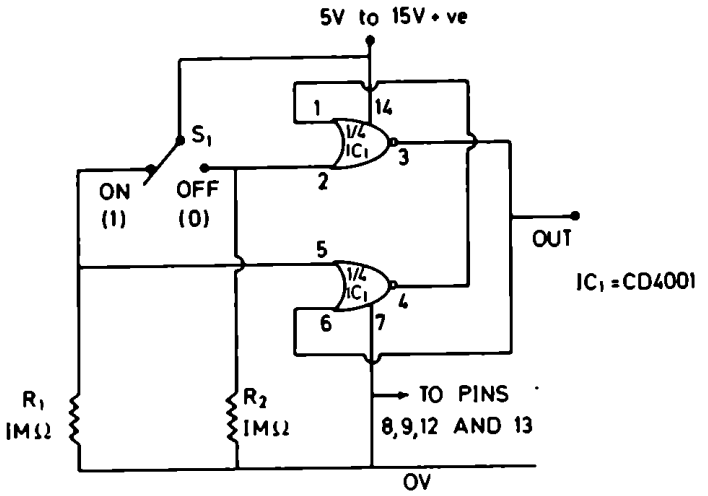


Figure 3.2 'Noiseless' ON/OFF switch

Figure 3.2 shows how the basic bistable multivibrator circuit of *Figure 3.1* can be modified for use as a 'noiseless' ON/OFF switch by deriving the input command signals from the positive supply line via a conventional ON/OFF switch.

A normal mechanical switch generates a good deal of noise (caused by point bounce, dirty contacts, etc.) when it is used to switch voltage or current, and this noise appears in the form of a series of high-amplitude voltage spikes at the start or end of the basic switching waveform. If a mechanical switch is coupled directly into a sensitive section of a high-speed pulse generating or counting circuit this noise can cause the circuit to malfunction. This snag can be overcome by using the *Figure 3.2* circuit to process the normal switching signals. The circuit's state is unaffected by noise, since its state is changed by the first noise pulse that occurs from the mechanical switching action, and cross-coupling then causes the circuit to self-latch and be immune to following noise pulses.

The basic bistable multivibrator of *Figure 3.1* is an electronically-triggered circuit. A manually-triggered bistable can be made by wiring normally-open push-button command switches between the positive supply line and the command input pins of the *Figure 3.1* circuit, as shown in *Figure 3.3*.

Alternatively, a manually-triggered bistable can be made by cross-coupling two NOT-connected gates of a CD4001, as shown in *Figure*

3.4. The operation of the circuit is basically similar to that of *Figure 3.1.* The output of the circuit sets to the logic 1 state when S_1 is momentarily closed, and resets at the logic 0 level when S_2 is momentarily closed. Note that, since both input terminals of each gate are

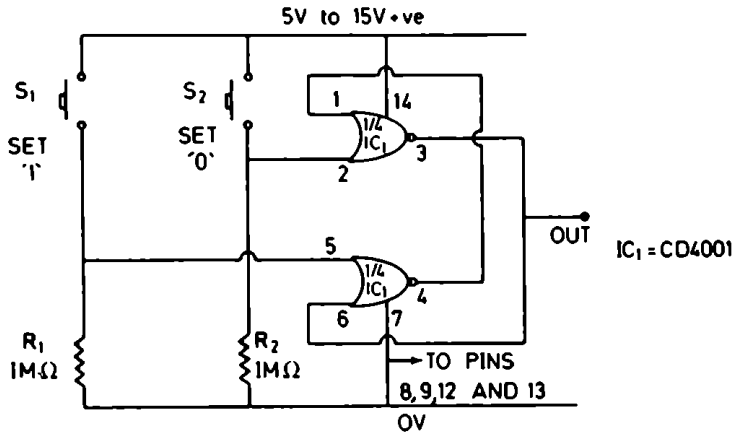


Figure 3.3 Manually-triggered bistable multivibrator

wired to the output terminals of their opposing gates via limiting resistors, the input terminals can be allowed to 'float' without having to be tied to ground via separate resistors.

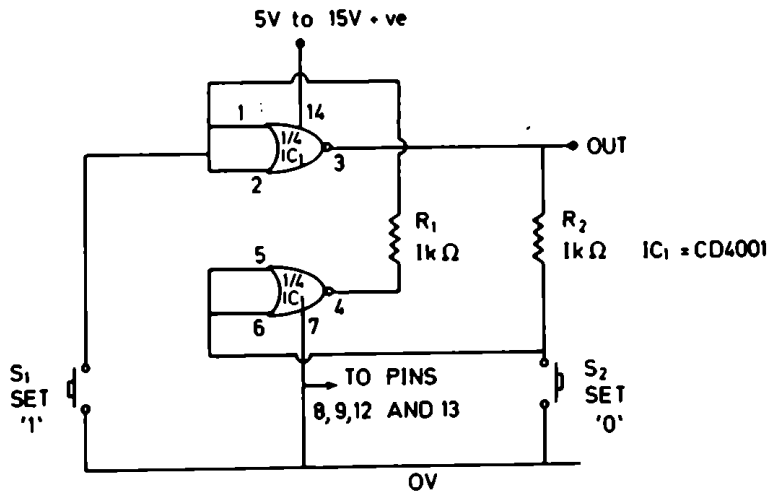


Figure 3.4 Alternative manually-triggered bistable

The four bistable circuits that we have looked at so far are very simple types, and have all been designed around the CD4001 COS/MOS IC. More advanced 'self-steering' counting and dividing bistable circuits can be built using a variety of more specialised COS/MOS digital ICs.

One such IC is the CD4013 dual 'D'-type flip-flop. *Figure 3.5a* shows the effective circuit and pin connections of this device, which is housed in a standard 14-pin dual-in-line package, and *Figure 3.5b* shows how the package can be wired so that it performs as a pulse-triggered frequency divider or counting circuit.

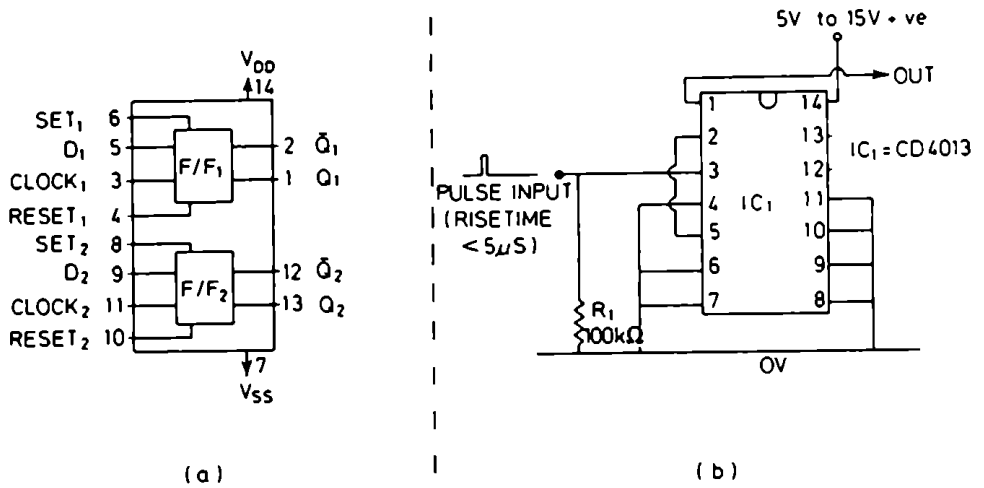


Figure 3.5a Effective circuit and pin connections of the CD4013 dual 'D'-type flip-flop. b Connections for making a pulse-triggered bistable frequency divider from one half of a CD4013

The *Figure 3.5b* circuit makes use of only one of the two available flip-flops within the CD4013 package, and the counting or 'toggle' action is obtained by connecting the Q_1 output to the data input, by shorting the set_1 and $reset_1$ inputs to ground, and by applying the pulse trigger input signals to the $clock_1$ input terminal. The action of the circuit is such that its output switches from one logic level to the other each time an input pulse is applied. If, for example, the output is initially at logic level 0, it will switch to logic level 1 on the arrival of the first input pulse, and then return to logic level 0 on the arrival of the second input pulse, and so on. The output frequency is thus half of that of the input signal, and the circuit acts as a divide-by-two counter.

The *Figure 3.5b* circuit is pulse-triggered, and its actual change of state is initiated during the positive-going transition of the clock pulse. The input trigger pulse should switch fully between the logic 0 and logic 1 levels, and must have a rise time of less than 5 μS.

If required, the above circuit can be triggered by non-pulse waveforms, such as sine or ramp signals, by simply feeding these input signals to the input of the bistable circuit via a wave-shaping Schmitt trigger circuit, as shown in *Figure 3.6.*

Finally, the *Figure 3.5b* circuit can be modified for manual triggering by using the connections shown in *Figure 3.7.* Here, manually-operated push-button switch S_1 is used to fire a monostable multivibrator, which generates a fast rise-time pulse which causes the bistable

to change state. The bistable thus changes state each time that S_1 is pressed. A detailed description of the operation of the monostable section of the circuit is given in the next section of this chapter.

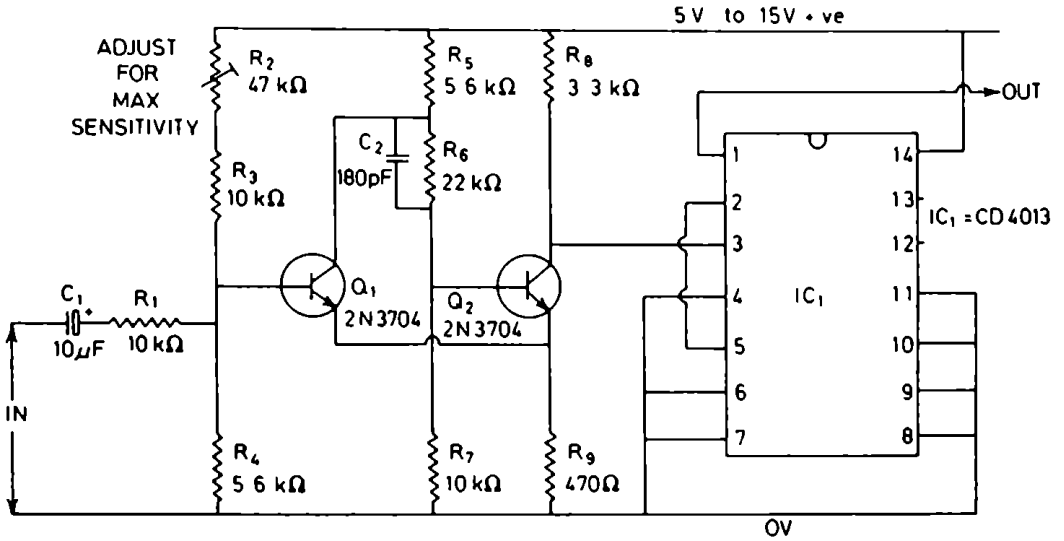


Figure 3.6 Bistable frequency divider that can be triggered by any input waveform.

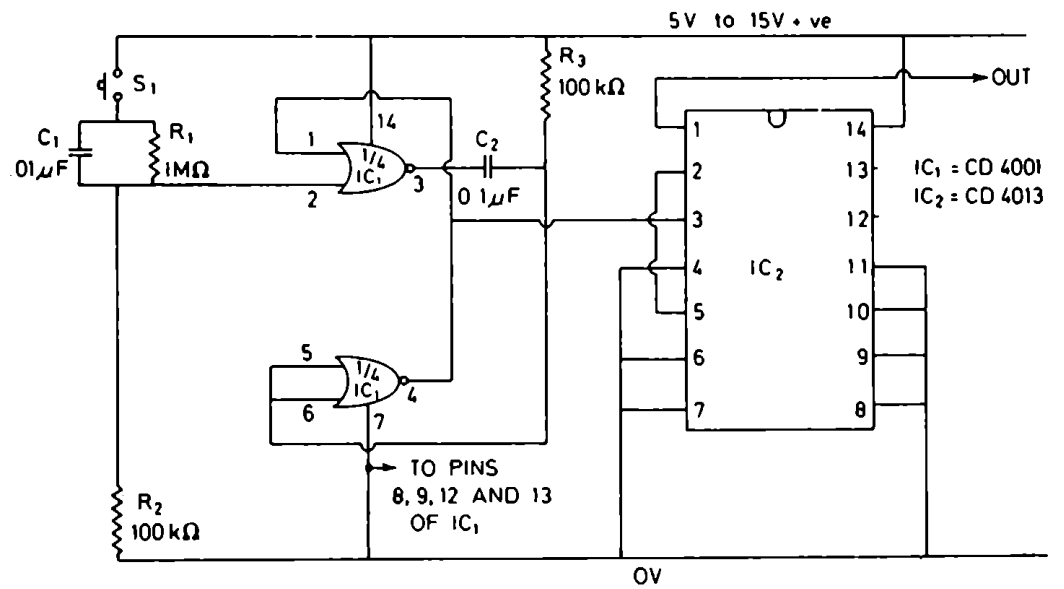


Figure 3.7 Manually-triggered bistable frequency divider.

Further applications of the CD4013 and other counting and dividing COS/MOS circuits are given in a later chapter of this volume.

Monostable multivibrator circuits

COS/MOS digital ICs such as the CD4001 offer considerable advantages when they are used in monostable multivibrator applications. In

particular, their general versatility enables monostable circuits to be designed with exceptionally good triggering characteristics, and their high input impedances enable long time constants to be obtained using large values of timing resistance and low values of timing capacitance.

A basic monostable or one-shot multivibrator can be made from two NOR logic gates by direct-coupling the output of one gate to the input of the other, and by coupling the output of the second gate to the input of the first via a simple R–C time-constant network. *Figure 3.8* shows a practical way of making a basic monostable multivibrator, or pulse stretcher, from one half of a CD4001 COS/MOS IC.

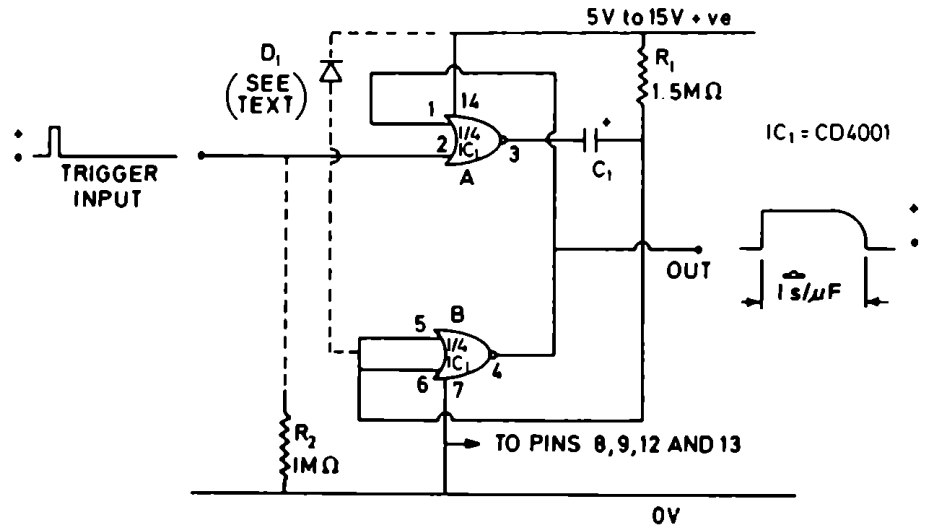


Figure 3.8 Basic monostable multivibrator or pulse stretcher.

Here, gate A is used as a NOR logic element, and gate B is used as an inverter or NOT gate. The circuit action is as follows.

Normally, when the circuit is in its quiescent state, the input to gate B is held high via R_1 and so the output at gate B is low. Both input terminals of gate A are thus low, and the output of gate A is high. Consequently, since both ends of C_1 are high, C_1 is fully discharged.

Suppose now that a brief positive trigger pulse is applied to the input of gate A. As soon as this pulse is applied it drives the output of gate A to ground, and drags the input of gate B with it via discharged capacitor C_1. Consequently, the output of gate B immediately goes high, and thus holds the output of gate A in the low state even when the input trigger pulse is subsequently removed.

As soon as the output of gate A goes low as the result of the applied trigger pulse, C_1 starts to charge via R_1, and an exponential rising voltage is applied to the input of gate B via the $R_1 - C_1$ junction. Eventually, after a delay determined by the R_1 and C_1 values, this

exponential voltage rises to the transfer voltage of gate B, and at this point the output of gate B switches sharply back into the low state, and the output pulse is terminated.

If the trigger input terminal is in the low state at this point of time, the output of gate A then switches back into the high state and C_1 discharges rapidly via the built-in D_1 input protection diode (see *Figure 1.10*) of gate B, and the operating sequence is complete. If, on the other hand, the input trigger terminal is still in the high state at this point of time, the output of gate A remains in the low state and C_1 continues to charge via $R_1 : C_1$ then discharges rapidly via D_1 when the input trigger terminal eventually goes to the low state. In either case, the duration of the ouput pulse is virtually independent of the state of the input trigger terminal.

Thus, the output of the *Figure 3.8* circuit is normally low, but changes to high as soon as a positive-going trigger signal is applied to its input. The output remains high for a certain period, and then switches abruptly back to the low state again. The precise period of the output pulse is determined by the R–C time constant, and by the value of the transfer voltage of the individual CD4001 IC that is used.

Four points should be noted about this simple but outstandingly useful circuit. The first point to note is that, since the time period of the circuit is dependent on the transfer voltage of the particular CD4001 IC that is used, the period obtained from a particular set of R–C values can vary considerably between one CD4001 and another. The CD4001 in fact has a production transfer voltage spread of 30% to 70% of the supply voltage.

In practice, the transfer voltage of any particular CD4001 is almost constant over a wide range of temperatures and supply voltages; thus the *Figure 3.8* circuit has excellent stability, but must have its time constant values individually adjusted to give a particular timing period. This circuit in fact gives a period of roughly 1 s/μF of C_1 value when R_1 has a value of 1.5 MΩ. C_1 can have any value between a few picofarad and hundreds of microfarad. The value of R_1 can range from a few thousand ohms to thousands of megohms, if required.

The second point to note about the circuit is that its input must always be tied to ground in the absence of a positive trigger pulse. This requirement can be met by applying the input from a d.c. source, or, if the input is a.c.-connected, by strapping the input terminal to ground via a resistor, as shown dotted by R_2 in the diagram.

The third point to note is that, since an exponential voltage is applied to the input of one of the gates during the operating cycle, the gate is driven into its linear region during each operating cycle. A measurable current thus flows in the circuit during the operating

period. All COS/MOS monostable and astable multivibrator circuits in fact pass a measurable current when they are in their functional modes.

The final and perhaps most important point to note concerns the triggering characteristics of the circuit. Its output pulse is actually initiated at the moment that the positive-going trigger input signal passes through the transfer voltage area of gate A, and the duration of the pulse is independent of the subsequent state of the trigger terminal. Consequently, the circuit can be triggered by any shape of input waveform, irrespective of its rise time or duration; the duration can be longer or shorter than that of the actual output pulse. The only requirement of the trigger signal is that its peak amplitude must exceed the transfer voltage of gate A. Thus, this simple monostable circuit has outstandingly good trigger characteristics.

The basic monostable circuit of *Figure 3.8* suffers from a couple of minor snags, but is still quite suitable for use in a number of simple

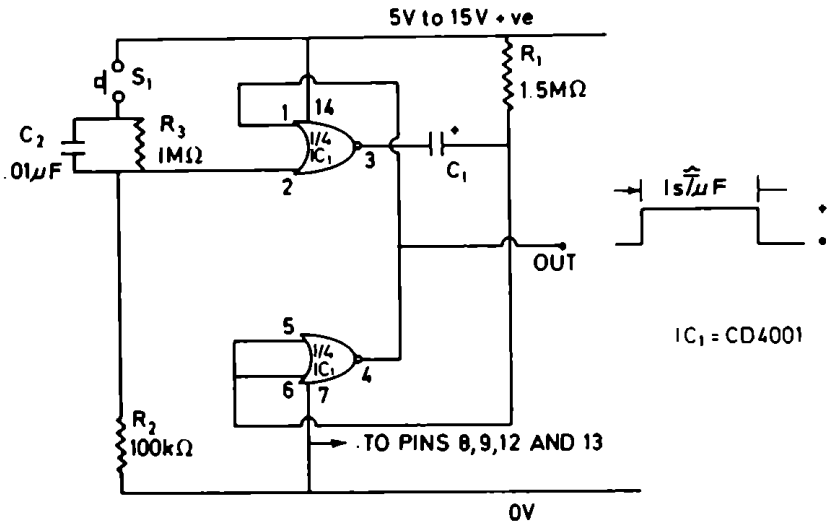


Figure 3.9 'Noiseless' push-button or manually-triggered monostable.

practical applications. *Figure 3.9*, for example, shows how the circuit can be used as a 'noiseless' push-button or manually-triggered monostable by simply using the push-button to apply a positive trigger pulse to the circuit via capacitor C_2: R_3 is used to discharge this capacitor when S_1 is released. The above circuit can also be described as an 'auto-turn-off time delay circuit', and gives a period of approximately 1s/μF of C_1 value.

One of the minor snags of the *Figure 3.8* circuit is that it has a relatively long recovery time, since C_1 has to discharge via the comparatively 'imperfect' built-in D_1 protection diode of gate B at the end of each pulse-generating cycle. In practice, this means that the pulse

length varies slightly with input frequency if the repetition period of the trigger signal is less than 10 times that of the output pulse. This snag can be overcome by simply wiring a general-purpose germanium signal diode between the positive supply line and the input terminals of gate B, as shown in *Figure 3.10*. This modification enables stable pulses to be developed even at repetition periods that are only fractionally longer than the output pulse period.

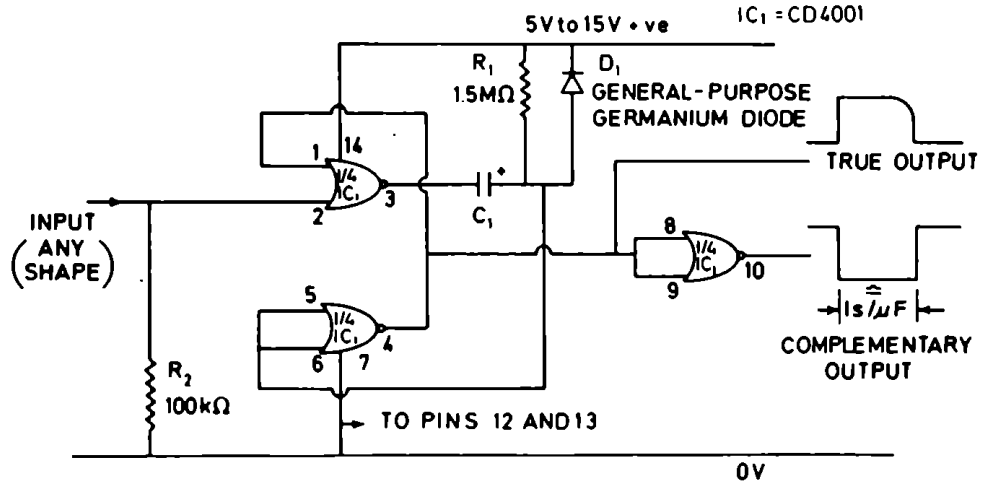


Figure 3.10 Modified mono with fast recovery and complementary output.

Figure 3.10 also shows how a complementary or anti-phase output can be obtained from the circuit by wiring one of the spare gates of the CD4001 as an inverter and connecting it between the output of the monostable and a separate output terminal.

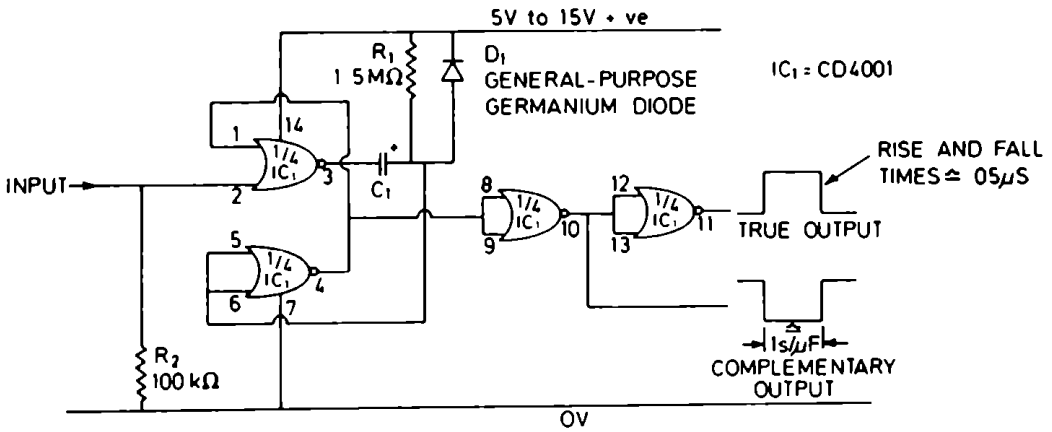


Figure 3.11 Improved monostable with true complementary output.

A second minor snag of the *Figure 3.8* circuit is that the trailing edge of its output pulse is slightly rounded. This snag can be overcome by wiring the remaining two gates of the CD4001 as a non-inverting pulse

amplifier and connecting this amplifier between the output terminals of the monostable and the final output terminals of the circuit, as shown in *Figure 3.11*. This final improved monostable multivibrator incorporates the fast recovery time modification, and gives true complementary outputs. The output pulses at the 'true output' terminals of the circuit have typical rise and fall times of about 0.05 μS.

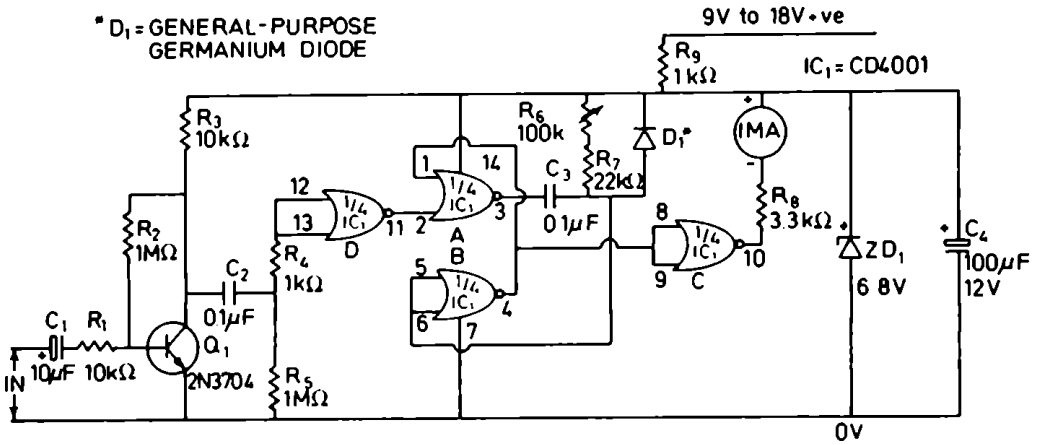


Figure 3.12 Simple 1 kHz linear-scale analogue frequency meter.

The modification and improved monostable multivibrator circuits of *Figures 3.10* and *3.11* have plenty of practical applications that are of general interest. *Figure 3.12*, for example, shows how the *Figure 3.10* circuit can be modified for use as a simple but highly accurate linearly-scaled analogue frequency meter, giving a full-scale reading of 1 kHz on an inexpensive 1 mA moving-coil meter.

Here, the input trigger signals are fed to the gate-A–gate-B monostable circuit via the Q_1 pre-amplifier and via the gate-D buffer stage, and the monostables output pulses are fed to the 1 mA meter via gate C and current-limiting resistor R_8. The supply rail of the circuit is stabilised at 6.8 V by the R_9–ZD_1–C_4 network. Consequently, a current pulse of fixed amplitude and fixed length is fed to the meter each time the monostable is fired.

Now, it can be shown that the mean current flowing in the meter in the above circuit is equal to the products of the peak pulse current and the pulse length and the repetition frequency of the pulse. In practice, the circuit gives a peak pulse current of approximately 2 mA and has a pulse length of 0.5 mS, so that the meter reads its full-scale value of 1 mA at 1 kHz, and reads 0.5 mA at 5000 Hz and 0.1 mA at 100 Hz. The circuit thus acts as a linear-scale frequency meter.

Note that the meter in this circuit cannot be damaged by applying too high an input frequency, since the maximum meter current is

limited to 2 mA by R_8, and all 1 mA moving-coil meters can withstand this magnitude of overload quite easily.

In practice, the *Figure 3.12* circuit can be made to read precisely 1 kHz at full scale by simply feeding an accurate 1 kHz signal to its input and adjusting R_6 for the full-scale reading. The linearity of the circuit is equal to that of the basic meter. The circuit can be triggered from any shape of input waveform, and has an input sensitivity of approximately 100 mV r.m.s. and an input impedance of about 10 kΩ.

The *Figure 3.12* circuit can be made to read alternative full-scale frequency values by altering the values of C_3 and/or R_6–R_7. Higher frequencies can be obtained by reducing the values of these components, and vice versa. The circuit gives a useful performance up to frequencies of a few hundred kilohertz.

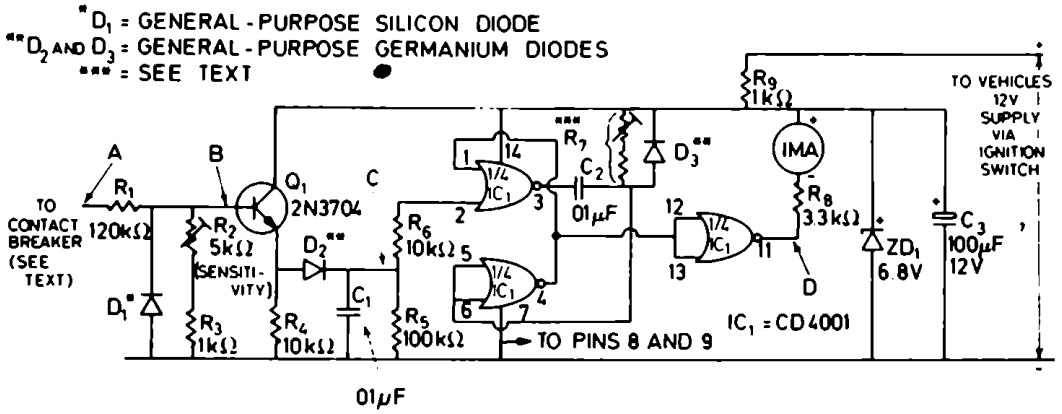


Figure 3.13a 12 V tachometer (rev/min meter) circuit for cars.

Figure 3.13a shows how the *Figure 3.10* circuit can be adapted for use as a tachometer or rev/min meter on cars fitted with 12 V electrical systems. Circuit operation relies on the fact that a vehicle's contact breaker develops a waveform with a basic frequency that is directly proportional to the engine's rev/min. In the *Figure 3.13a* circuit this waveform is picked up and used to fire a monostable multivibrator and give a reading on a 1 mA meter, in a way similar to the *Figure 3.12* circuit, but in this case the meter is calibrated in rev/min rather than in frequency.

The interesting technical feature of the *Figure 3.13a* circuit is the method of converting the basic contact-breaker signal into a form suitable for triggering the COS/MOS monostable multivibrator. *Figure 3.13b* shows the actual waveforms obtained in different parts of the circuit when fitted to a 4-cylinder car at 3000 rev/min. Note particularly the details of the contact-breaker signal appearing at point 'A' of the circuit.

As the contact breaker first opens, the ignition coil is thrown into oscillatory action at a frequency of approximately 10 kHz. In the first half-cycle of this action a peak voltage of about 250 V is developed

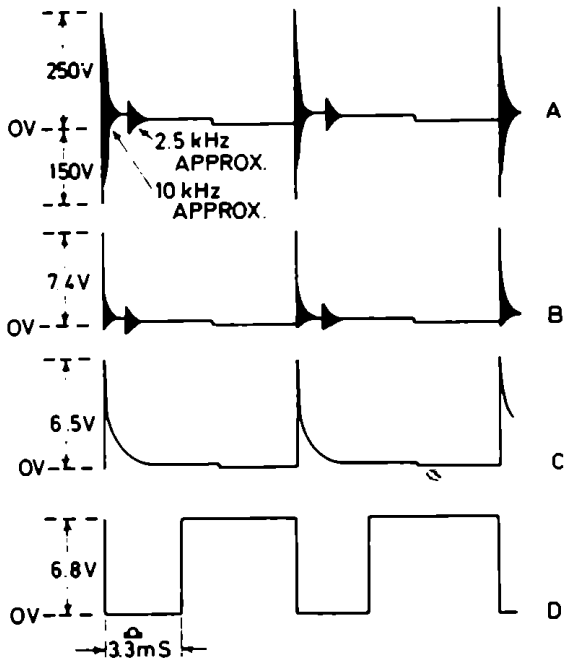


Figure 3.13b Waveforms obtained in different parts of the tachometer circuit when fitted to a 4-cylinder car at 3000 rev/min.

across the contact breaker, but this peak amplitude drops rapidly to about 30 V as ionisation takes place across the vehicle's spark-plug gap. After 1.5 mS or so the ionisation process ceases, and the coil again goes into oscillation, this time at a frequency of about 2.5 kHz; as this oscillation dies away the contact-breaker voltage stabilises at the vehicle's battery voltage of roughly 12 V. Eventually, the contact breaker closes again and the voltage falls to zero. When the contact breaker re-opens another high-voltage oscillatory action is initiated, and the waveform repeats.

Thus, the contact-breaker signal is quite complex, and contains a variety of frequency and voltage components. To trigger our tachometer, we need to detect the basic contact-breaker frequency, but reject all transient oscillatory voltages. In the *Figure 3.13a* circuit this is achieved as follows.

First, the basic contact-breaker signal is applied to the base of emitter follower Q_1 via potential divider R_1–R_2–R_3 and rectifier diode D_1. The potential divider reduces the magnitude of the signal by a factor of about 40, and the diode eliminates the negative parts of the signal at point 'B' of the circuit. Any positive parts of the signal at

point 'B' that significantly exceed the 6.8 V zener-stabilised supply of Q_1 cause the base-collector junction of the transistor to become forward biased, so positive signals are automatically clipped at about 7.4 V at point 'B' of the circuit.

The signal appearing at the emitter of Q_1 is similar to that of the base, except that approximately 600 mV is subtracted from all parts of the waveform by the forward-biased base-emitter junction of the transistor. This waveform is fed to a peak-detecting time-constant circuit formed by D_2–C_1 and R_5, with the result that a pulse waveform, with a short rise time and relatively long fall time, is developed at point 'C' of the circuit. This waveform is used to trigger the monostable multivibrator via R_6.

Note that, since the monostable is fired by a positive-going transition voltage with a nominal value of 3.4 V (= 50% of the 6.8 V supply voltage), and since the input attenuator gives a division factor of about 40, the monostable actually fires at the moment that the contact-breaker signal rises to approximately 126 V as the points first open.

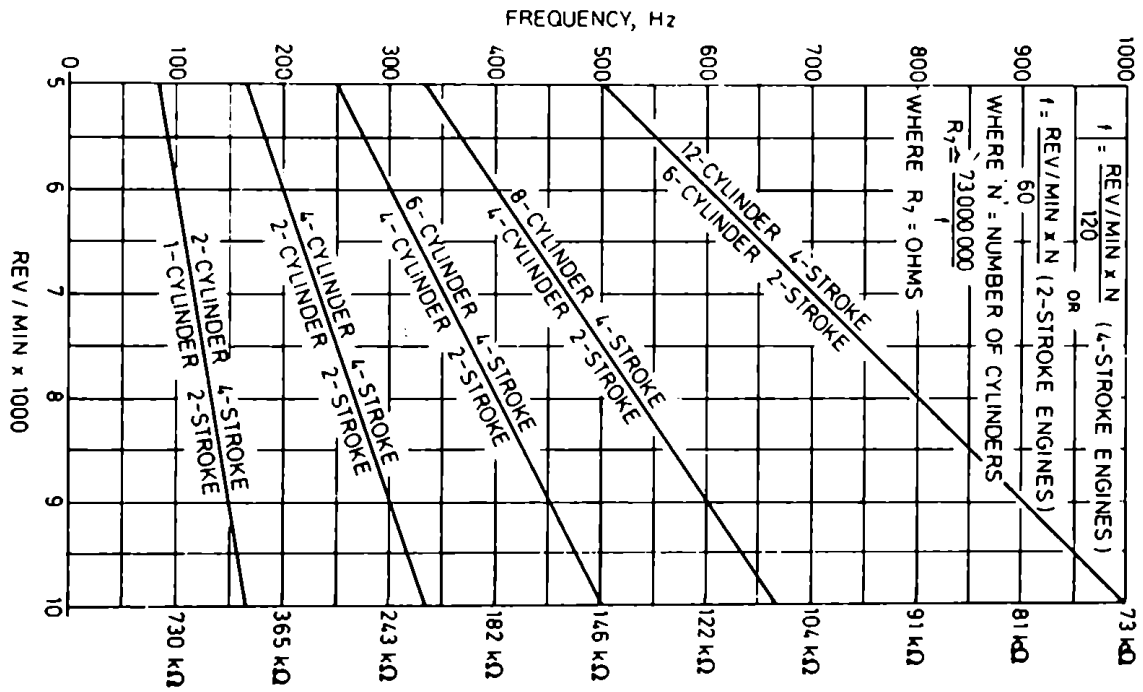


Figure 3.13c Relationship between f, rev/min, and R7 value needed for f.s.d. tachometer readings on different types of engine.

The monostable is thus fired in synchrony with the contact breaker, but is unaffected by voltage transients with magnitudes lower than 126 V or so. The *Figure 3.13a* circuit thus acts as a versatile and accurate tachometer or rev/min meter.

The tachometer circuit can be fitted to any vehicle having a 12 V electrical system, irrespective of the system's polarity. The unit's supply leads are simply connected to the vehicle's battery via the ignition switch, and the circuit's input terminal is taken to a suitable pick-up point. On vehicles with conventional ignition systems, the terminal is taken to the contact breaker. On vehicles fitted with capacitor-discharge ignition systems the terminal should be connected to the high-voltage output point of the C–D unit.

Before fitting the unit to the car, it must first be calibrated to give the appropriate full-scale rev/min readings for the particular vehicle in question. The procedure here is to first decide the full-scale rev/min reading that is required, and then consult the graph of *Figure 3.13c* to find the frequency that corresponds to that reading on that particular vehicle. Thus, a frequency of 333 Hz corresponds to a reading of 10 000 rev/min on a 4-cylinder 4-stroke engine. A square-wave or pulse of this frequency, with a peak amplitude of approximately 6.8 V, must then be connected across the R_2–R_3 combination via a 1 kΩ limiting resistor, after first setting R_2 to maximum value, and R_7 is then adjusted to give the full-scale reading on the meter. The calibration procedure is then complete.

Note that R_7 comprises a fixed and a variable resistor in series. The graph of *Figure 3.13c* shows the approximate total value of R_7 that is needed to give full-scale meter readings at particular frequencies when C_2 has a value of 0.01 μF. Note that, if preferred, C_2 can be increased to 0.1μF and the R_7 value can then be reduced by a factor of ten.

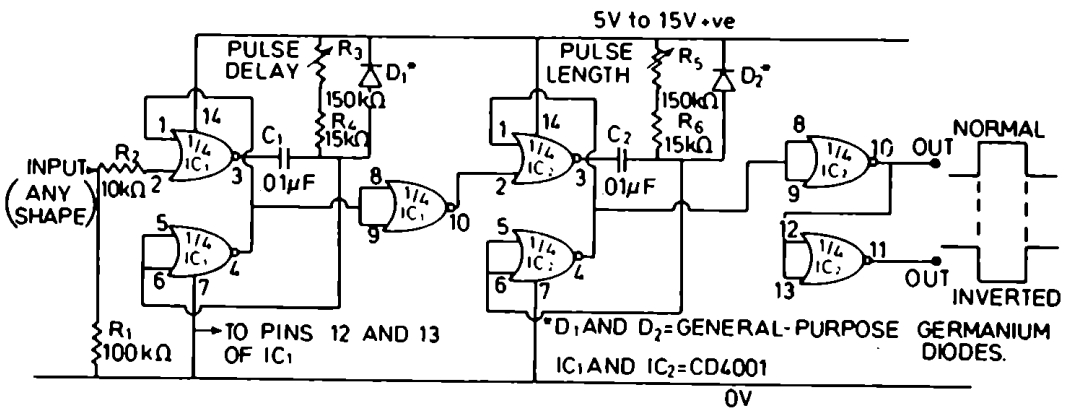


Figure 3.14 Delayed-pulse generator, covering the range 0.1 to 1 mS

Once the unit has been fitted to the car, the value of 'sensitivity' control R_2 should be reduced to slightly above the minimum value at which triggering can be reliably obtained without interference from spurious signals. The setting-up procedure is then complete, and the unit is ready for use.

Finally, *Figure 3.14* shows how the circuits of *Figures 3.10* and *3.11* can be combined to form a delayed pulse generator, which delivers a pulse of adjustable length a pre-set time after the application of the initial trigger pulse.

Here, the input trigger signal is applied to the monostable multivibrator formed by IC_1, which fires as soon as the trigger signal is applied. The output of this monostable is inverted and fed to the input of the second monostable multivibrator, which turns on at the moment that the first monostable turns off. Thus, the triggering of the final output pulse is delayed by an amount determined by the period of the first monostable.

In practice, both the delay and pulse-length periods of the *Figure 3.14* circuit can be varied over the approximate range 0.1 mS to 1.0 mS using the component values shown. Alternative delay periods and pulse lengths can be obtained by simply changing the values of the C_1–C_2 time-constant capacitors. The periods are directly proportional to the capacitor values, and can be increased by raising the values, or reduced by lowering the values.

The circuit gives both direct and inverted output pulses, and can be triggered by any shape of input trigger signal. If required, a variable-frequency triggering section can be built into the *Figure 3.14* design in the form of one of the COS/MOS astable multivibrator circuits described later in this chapter, thus forming a complete and versatile variable pulse generator from only three CD4001 ICs.

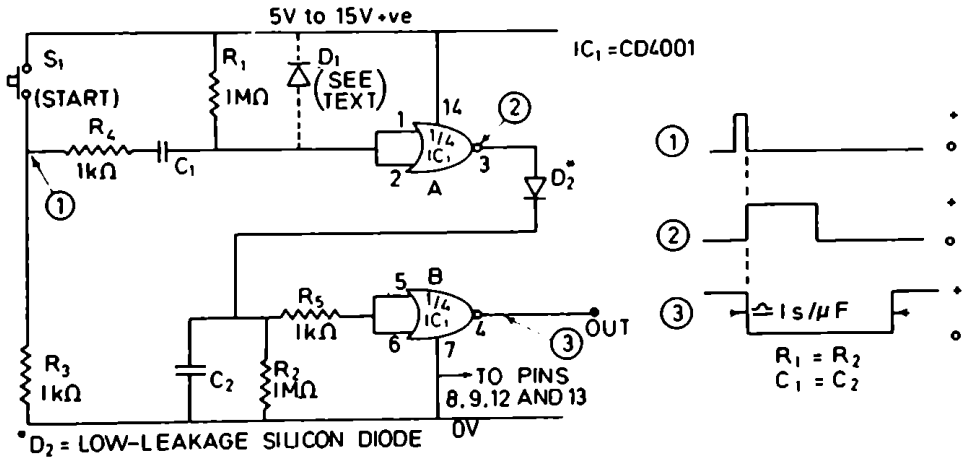


Figure 3.15 Basic compensated monostable multivibrator

The circuits of *Figures 3.8* to *3.14* are all variants of the 'basic' COS/MOS monostable multivibrator. It has already been pointed out that, although this circuit gives a performance that is excellent for many purposes, a major disadvantage of this design is that its period depends on the transfer voltage value of the individual COS/MOS IC that it is used

with, and is not dictated solely by its R–C time-constant value. *Figure 3.15* shows the basic circuit and waveforms of a 'compensated' monostable multivibrator that does not suffer from this snag. Note that the circuit used two sets of R–C time-constant components. Circuit operation is as follows.

When the circuit is in its quiescent state the S_1 side of C_1 is grounded via R_3, but the R_1 side is held positive. C_1 is thus fully charged under this condition, and the input of gate A is high. The output of gate A is thus low, so C_2 is fully discharged at this time, and the output of gate B is high.

Suppose now that START button S_1 is briefly closed and then released. As S_1 is closed, the S_1 end of C_1 is connected to the positive supply line, and C_1 discharges rapidly via R_4 and D_1 (which is one of the input protection diodes built into the CD4001). This action has no effect on the circuit. When S_1 is released, however, C_1 is fully discharged, so as soon as S_1 is released C_1 starts to recharge via R_1, R_3, and R_4, thus pulling the input of gate A low and making the output of gate A go high. As the output of gate A goes high it charges C_2 rapidly via D_2, and thus causes the output at gate B to go low.

As soon as S_1 is released, C_1 starts to charge up, and a rising exponential voltage is applied to the input of gate A. After a time determined by the R_1 and C_1 values this voltage *rises* to the transfer voltage of gate A, and at this point the output of gate A switches sharply into the low state and removes the charging voltage from C_2 as D_2 becomes reverse biased. C_2 then starts to discharge via R_2, and after a time determined by the R_2 and C_2 values the C_2 voltage *falls* to the transfer voltage of gate B, and at this point the output of gate B switches sharply into the high state. The operating sequence of the circuit is then complete. Note that R_4 and R_5 are used purely as safety resistors, and prevent heavy capacitor discharge currents from flowing into the IC gates if power is removed from the circuit during the operating sequence.

Now, this particular circuit uses two identical R–C time-constant networks, and its final output period is equal to the sum of the two individual time constants. The important point to note, however, is that one of these time constants causes a circuit action when its exponential voltage *rises* to the transfer voltage of gate A, and the other causes a circuit action when its voltage *falls* to the transfer voltage of gate B. Consequently, if both gates have identical transfer voltages, the transfer voltage values effectively cancel out, and have no effect on the actual period of the circuit.

Although transfer voltage values can vary over wide limits between individual COS/MOS ICs, the individual transfer voltage values of a set

of gates within a single CD4001 IC are always virtually identical, since the gates are all formed on the same semiconductor chip at the same time. Consequently, the total timing period of the *Figure 3.15* circuit is dictated purely by the values of R_1–C_1 and R_2–C_2, and is independent of variations in the parameters of individual CD4001 ICs.

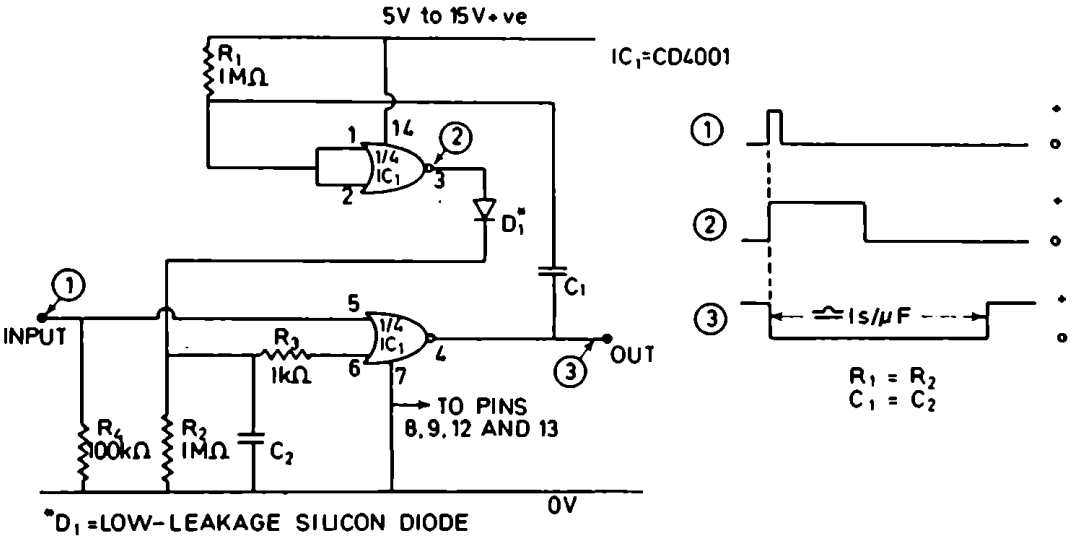


Figure 3.16 Improved compensated monostable multivibrator

The *Figure 3.15* circuit is shown as being manually triggered. The circuit can be modified for electronic triggering by simply eliminating S_1 and applying the positive trigger pulse across R_3. In either case, a

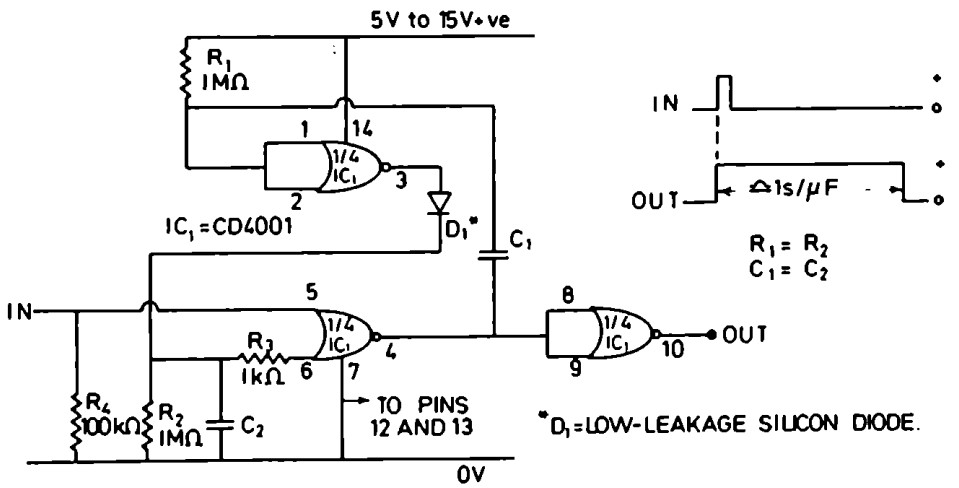


Figure 3.17 Positive-output compensated monostable multivibrator

practical disadvantage of this simple circuit is that the actual monostable action is initiated by the end, rather than the start, of the input trigger pulse. This snag can be overcome by modifying the circuit as shown in *Figure 3.16*.

The *Figure 3.16* circuit gives an output that is normally high (positive), but which goes low (to OV) for a pre-set period when a trigger pulse is applied. If required, the polarity of the output signal can be reversed, so that it is normally low but goes high for the duration of the output pulse, by simply wiring an inverter into the output of the circuit, as shown in the positive-output compensated monostable circuit of *Figure 3.17*.

Astable multivibrator circuits

The most widely used type of multivibrator circuit is the astable, or square-wave generator. *Figure 3.18* shows how one half of a CD4001 COS/MOS IC can be used to make a basic 1 kHz astable multivibrator.

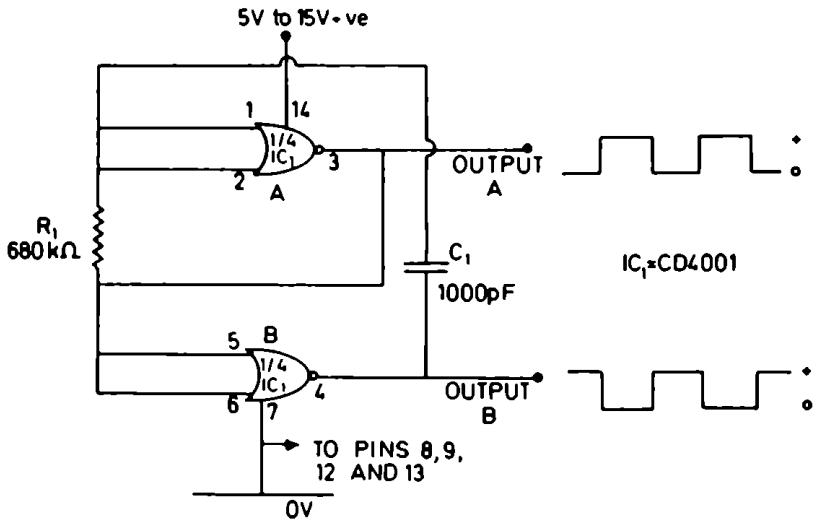


Figure 3.18 Basic 1kHz astable multivibrator or square-wave generator

Note that both gates of the circuit are connected as simple inverters, and that the circuit uses only a single set of R–C time-constant components. The action of the circuit is as follows.

Suppose initially that a state has been reached in the circuit operation where the output of gate B has just switched into the high state and the output of gate A has just switched into the low state, and that C_1 is fully discharged at this moment.

Since C_1 is discharged at this time, the input of gate A is effectively shorted to the output of gate B, and is high. As soon as the above state of operation is obtained, C_1 starts to charge up via R_1 and the low

(effectively grounded) output of gate A, and the voltage at the input of gate A (which is derived from the R_1–C_1 junction) starts to decay exponentially towards zero.

Eventually, after a delay determined by R_1 and C_1, the input voltage of gate A falls to the transfer voltage point of gate A, and at this instant the output of gate A switches into the high state and drives the output of gate B into the low state. As the output of gate B switches to the low state it forces the positive end of C_1 downwards, and thus forces the gate A input end of C_1 to attempt to swing negative with respect to the OV line. As the input of gate A goes negative to the OV line input protection diode D_3 (see *Figure 1.10*) conducts and removes the charge from C_1.

Thus, at the end of this switching cycle C_1 is again fully discharged, the output of gate B and the input of gate A are low, and the output of gate A and the input of gate B are high.

As soon as this new stage of the operation is obtained, C_1 starts to recharge in the reverse direction via R_1 and the low (grounded) output of gate B, and the voltage at the input of gate A (which is derived from the R_1–C_1 junction) starts to rise exponentially towards the positive rail voltage. Eventually, after another delay determined by R_1 and C_1, the input voltage of gate A rises to the transfer voltage of the gate, and at this instant the output of gate A switches into the low state and drives the output of gate B into the high state. At this moment C_1 discharges rapidly via the D_1 input protection diode (see *Figure 1.10*) of gate A as the R_1–C_1 junction end of the capacitor attempts to go positive relative to the positive supply line, and the operating sequence is then complete. The switching sequence then repeats *ad infinitum*, and a series of approximately square waves are generated at the two outputs of the circuit. Output A is in anti-phase relative to output B.

An outstanding feature of the basic astable multivibrator circuit of *Figure 3.18* is that it uses only two time-constant components (R_1 and C_1), and the values of both of these components can be varied over wide ranges to give required operating frequencies. The value of R_1 can be varied from a few thousand ohms to thousands of megohms, and C_1 (which must be a non-polarised capacitor) can be varied from a few picafarad to hundreds of micofarad. The operating frequency is inversely proportional to the R_1 and C_1 values, and can be varied from less than one cycle per hour to several megahertz.

The operating frequency of the basic circuit can be made variable, if required, by wiring a variable resistor in series with limiting resistor R_1, as shown in the circuit of *Figure 3.19*. With the component values shown, this circuit covers the approximate frequency range 600 Hz to 6 kHz.

Figure 3.20 shows how the basic astable multivibrator can be modified for use as a manually-activated multitone oscillator. Here, tone-determining resistors R_1 to R_3 are connected in the circuit via normally-open push-button switches S_1 to S_3, thus enabling the circuit to be

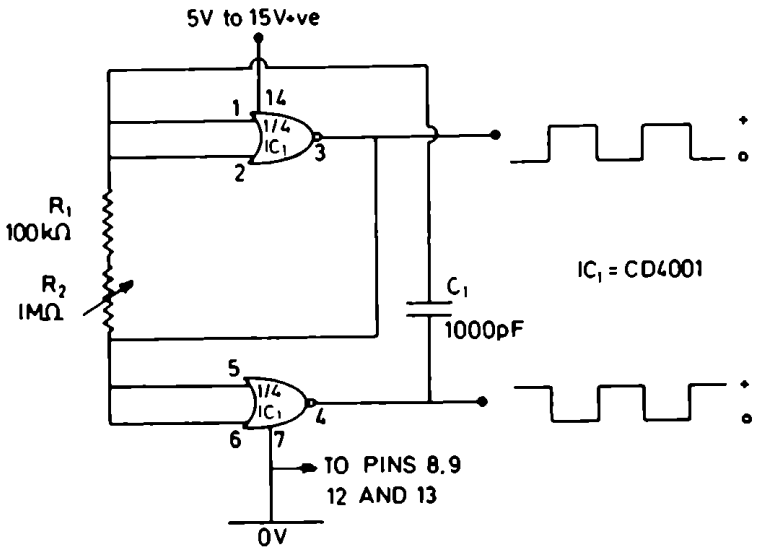


Figure 3.19 Variable-frequency (600 Hz - 6 kHz) astable multivibrator

activated at the required tones. Note that resistor R_4 is wired between ground and the input of gate A, to ensure that the gates maintain stable states when all of the tone-selecting push buttons are open. The value

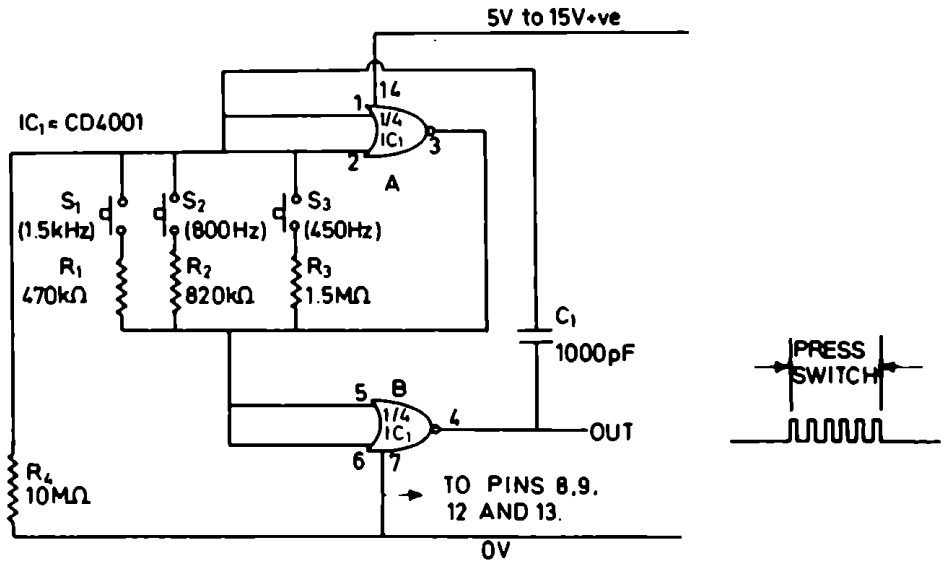


Figure 3.20 Manually-triggered multi-tone astable multivibrator

of R_4 must be large relative to the value of the largest of the tone-determining resistors, so as not to impair the oscillatory action of the circuit.

If required, the basic astable multivibrator of *Figure 3.18* can be gated on or off via an external pulse signal by connecting gate A as a NOR gate and applying the gating signal to one of the NOR gate inputs, as shown in *Figure 3.21*. The multivibrator is cut off when the gate input signal is high, and is operative when the gate input signal is low.

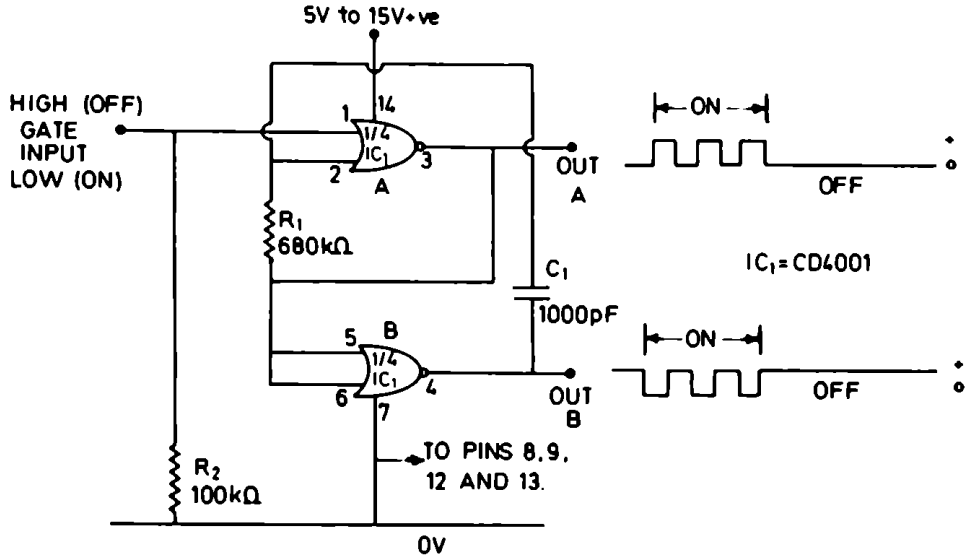


Figure 3.21 Gated 1 kHz astable multivibrator

The basic astable multivibrator of *Figure 3.18* acts as a simple and very useful circuit, but suffers from several disadvantages. The first of these is that, since the voltage swing of C_1 is clamped to the limits of

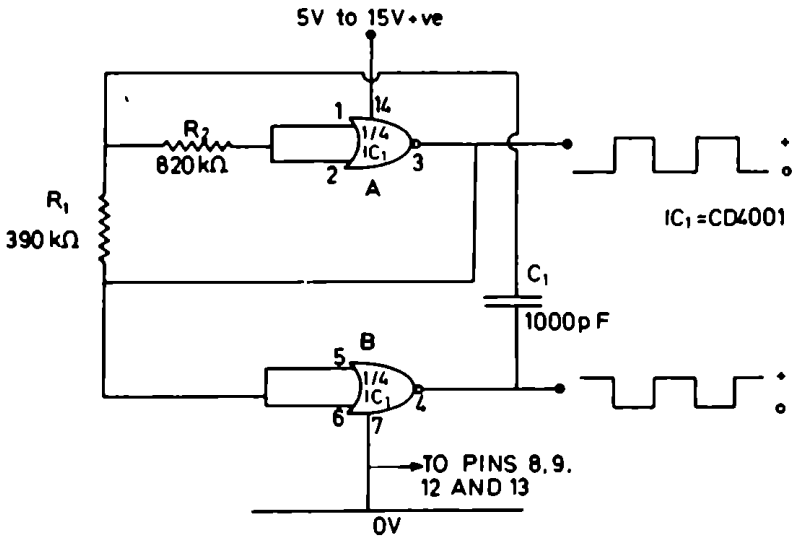


Figure 3.22 Compensated 1 kHz astable multivibrator

the power supply voltage by the input protection diodes of the COS/MOS gates, the operating frequency is influenced by variations in the

supply rail voltage. Typically, a 40% variation in supply voltage causes a 5% variation in frequency.

Another disadvantage is that the frequency of operation is influenced by the transition voltage values of the CD4001 COS/MOS gates, and in practice the actual frequency of operation may vary by 10% over the production spread of the CD4001 when using identical R_1 and C_1 values.

Both of these disadvantages can be largely overcome by simply wiring a high-value resistor in series with the input of gate A, as shown in *Figure 3.22*, thus enabling the voltage swing of C_1 to exceed the supply rail voltage. Limiting resistor R_2 must have a value at least double that of timing resistor R_1. The operating frequency is influenced by the values of both of these resistors.

In practice, the operating frequency of the *Figure 3.22* circuit is subject to a change of less than 5% over the production spread of transfer voltages, and to a frequency shift of less than 2% with a 40% change in supply voltage. Another advantage conferred by the use of R_2 is that of excellent thermal stability. The operating frequency typically varies by only 1% over the temperature range –40°C to +85°C.

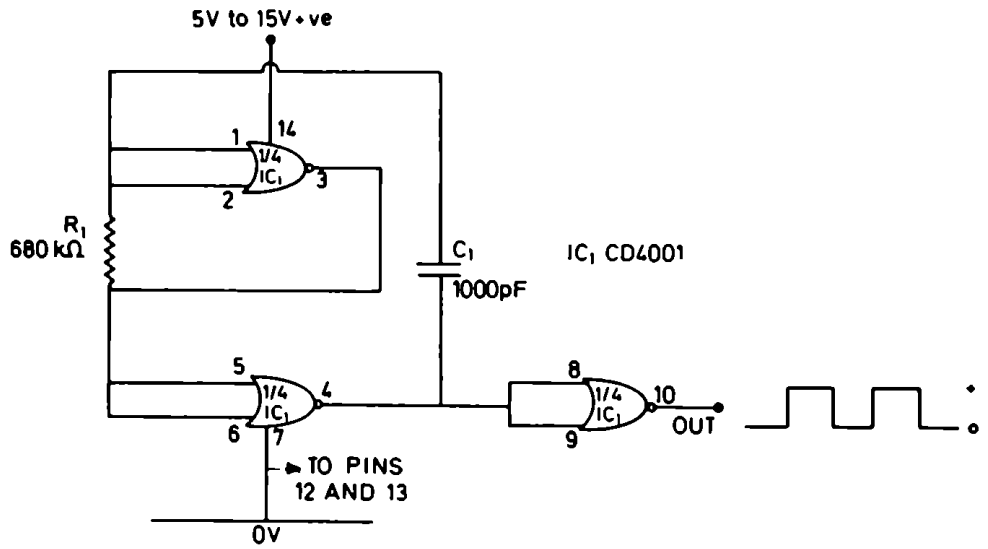


Figure 3.23 Buffered-output 1 kHz astable multivibrator

Minor disadvantages of both the basic and the compensated astable circuits are that the leading and trailing edges of their output waveforms sometimes contain a certain amount of 'sag and mush', and the operating frequency is influenced by variations in the output loading conditions. Both of these disadvantages can be overcome by interposing

an inverting buffer stage between the output of the astable multivibrator and the input of the external loading circuit, as shown in *Figure 3.23.*

A final disadvantage of the basic astable circuit, and to a lesser degree of the compensated circuit, is that the symmetry or mark/space ratio of the output waveform depends on the transition voltage value of the individual CD4001 IC that is used. An IC with a transition voltage value of 35% gives a mark/space ratio of approximately 35/65, and an IC with a value of 60% gives a mark/space ratio of approximately 60/40. A true square-wave (50/50) output is available only if the IC has a transition voltage value of exactly 50%.

The mark/space ratio of the output waveform of the astable circuit can be made variable by using steering diodes to select alternative charge and recharge resistance paths for the time-constant network, as shown in *Figure 3.24* and *3.25*.

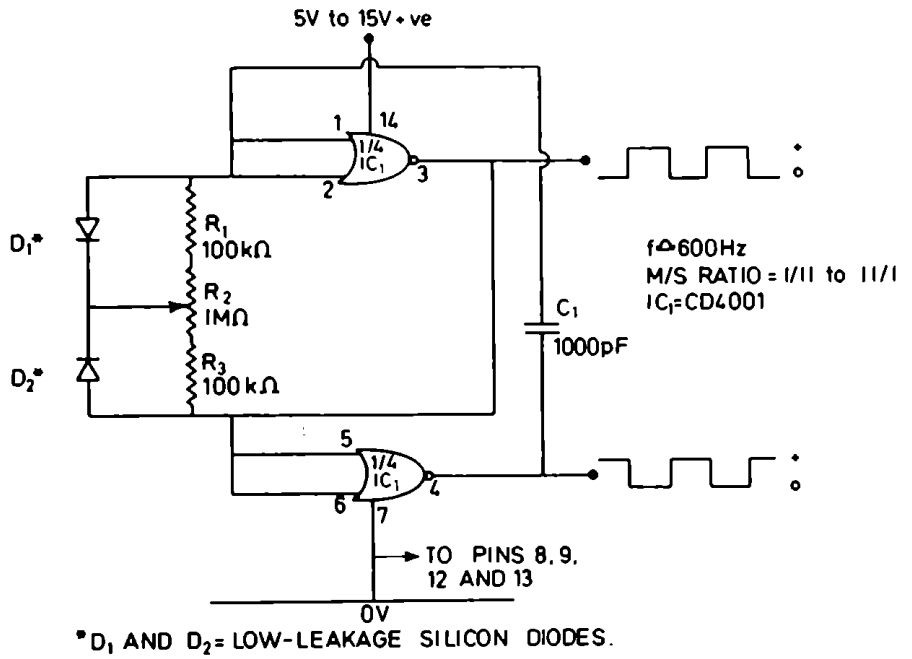


Figure 3.24 Variable mark/space ratio astable multivibrator

In the *Figure 3.24* circuit the capacitor charges via D_1 and the low half of the resistance chain in one half-cycle, and via D_2 and the top half of the resistance chain in the other half-cycle. The mark/space ratio can be varied over the range 1/11 to 11/1 via R_2, and the circuit operates at a frequency of roughly 600 Hz: the frequency varies slightly as the mark/space ratio is varied.

Finally, the *Figure 3.25* circuit has independently variable ON and OFF times. In one half-cycle the capacitor charges via $D_1 - R_1$ and R_3, and in the other half-cycle it charges via $D_2 - R_2$ and R_4. The

period of each half-cycle is variable over the approximate range 8 μS to 800 μS using the component values shown. Periods of up to one hour can be obtained by increasing the component values.

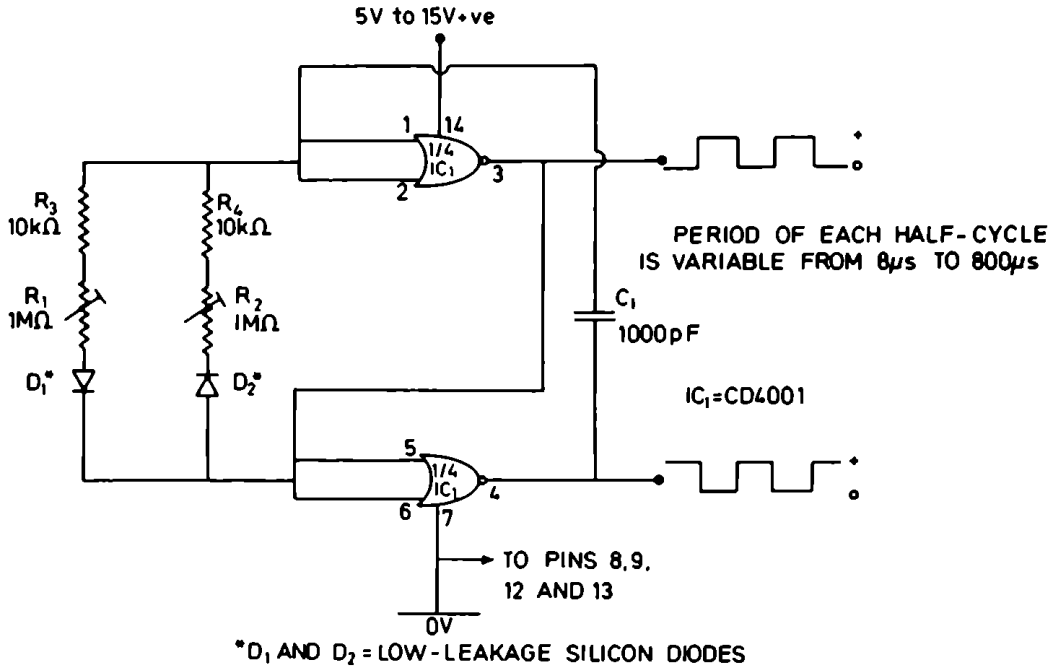


Figure 3.25 Astable multivibrator with independently variable on and off times.

In following chapters of this volume, we show many practical applications of the different types of multivibrator circuit that we have discussed here.

CHAPTER 4

10 D.C. LAMP-CONTROL CIRCUITS

The ubiquitous CD4001 quad 2-input COS/MOS NOR gate has a multitude of practical applications in gadgets for the home and the car. A typical example is in d.c. lamp-control applications. Here, the CD4001 can be used as the basis of a number of manually or automatically activated lamp flashers, and in lamp-dimming and lamp-switching circuits. In the present chapter we show ten such applications.

D.C. lamp-flasher circuits

Figure 4.1 shows how one half of a CD4001 IC can be used in conjunction with a couple of transistors to make a simple lamp-flasher circuit that drives a 12 V lamp on and off at a rate of approximately 1.5 seconds per flash, or 40 flashes per minute.

Here, one half of the CD4001 is wired as a simple astable multivibrator, with its output feeding to the lamp via Q_1 and Q_2. Power is applied to the circuit via switch S_1. When the astable multivibrator is operating, its output switches alternately between OV and the full positive supply voltage. When the output of the astable is at OV, transistors Q_1 and Q_2 are driven on via R_2, and the lamp is illuminated. When the output of the astable is at full positive supply voltage, zero bias is applied to the transistors, and Q_1–Q_2 and the lamp are off. Thus, the lamp flashes on and off at a rate determined by the astable circuit.

The simple lamp-flasher circuit of *Figure 4.1* can be modified in a number of ways to meet individual requirements. The basic circuit, for example, is intended for use in applications where one side of the lamp

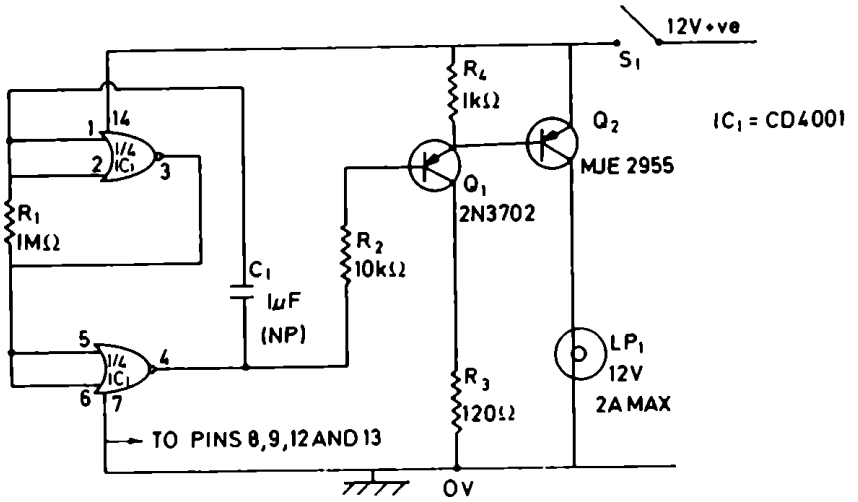


Figure 4.1 Simple d.c. lamp flasher (rate ≙ 1.5 seconds per flash, ≙ 40 flashes per minute)

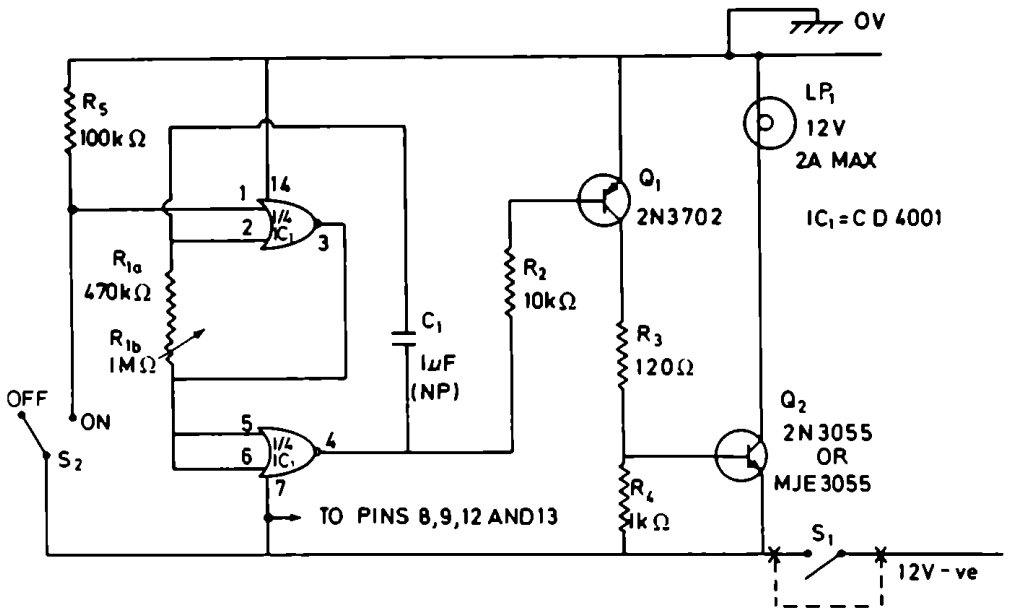


Figure 4.2 Modified d.c. lamp flasher (Rate ≙ 0.75 to 2.25 seconds per flash, ≙ 80 to 27 flashes per minute)

is taken to the grounded 'negative' line, as in the case of negative-ground cars. *Figure 4.2* shows how the connections of Q_1 and Q_2 can be modified for use in applications where one side of the lamp goes to the grounded 'positive' line, as in the case of positive-ground cars. Note that S_1 (the ON/OFF switch) is wired in the negative line in this case.

If required, S_1 can be shorted out (as shown dotted in the diagram) and the circuit can be gated ON and OFF via R_5 and pin 1 of the CD4001, and via low-current switch S_2. In this case the circuit passes a typical standby or leakage current of 1 mA via Q_2 when S_2 is in the OFF position.

The *Figure 4.2* circuit also shows how the flashing rate can be made variable by replacing R_1 with a fixed 470 kΩ resistor and a variable 1 MΩ resistor, as shown by R_{1a} and R_{1b}. In this case the rate can be varied from approximately 27 to 80 flashes per minute via R_{1b}.

The *Figures 4.1* and *4.2* circuits are intended for use with any 12 V lamps with current ratings up to a maximum of 2 A. The circuits can be used with lamps having current ratings up to about 6 A by simply using a third (medium-power) transistor, wired between the base and collecter of Q_2, so that the combination acts as a high-gain Darlington or Super-Alpha pair.

The two lamp-flasher circuits that we have looked at so far have duty cycles or mark/space ratios of approximately 1 : 1, so that the lamps turn on and off for approximately equal times.

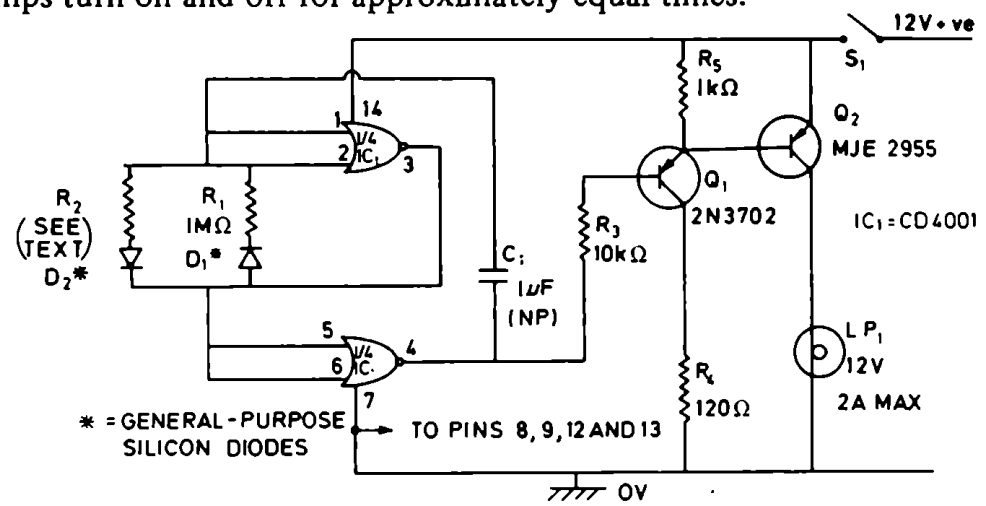


Figure 4.3 Programmed-duty-cycle (P-D-C) lamp flasher

Figure 4.3 shows how the circuits can be modified to give a programmed duty cycle so that, for example, the lamps turn on for a single period of only 0.75s in each 8.25 second cycle, thus giving a 1 : 10 duty cycle and giving considerable current economy as an emergency lamp flasher. The ON time of the lamp is controlled by R_1 and D_1, and is fixed at about 0.75s, but the OFF time is controlled by R_2 and D_2, and can be varied over a wide range. When R_2 is given a value of 1 MΩ the lamp has an OFF time of 0.75s, and when R_2 has a value of 10 MΩ the OFF time is about 7.5s. The R_2 value can be varied from a few thousand ohms to thousands of megohms, as required, to give any desired OFF time.

The *Figure 4.3* circuit is intended for use in applications where one side of the lamp and the negative terminal of the supply battery are both taken to a common ground point, as in negative-ground cars. The ON/OFF switch of the circuit is wired in series with the positive supply lead, and passes the full lamp current.

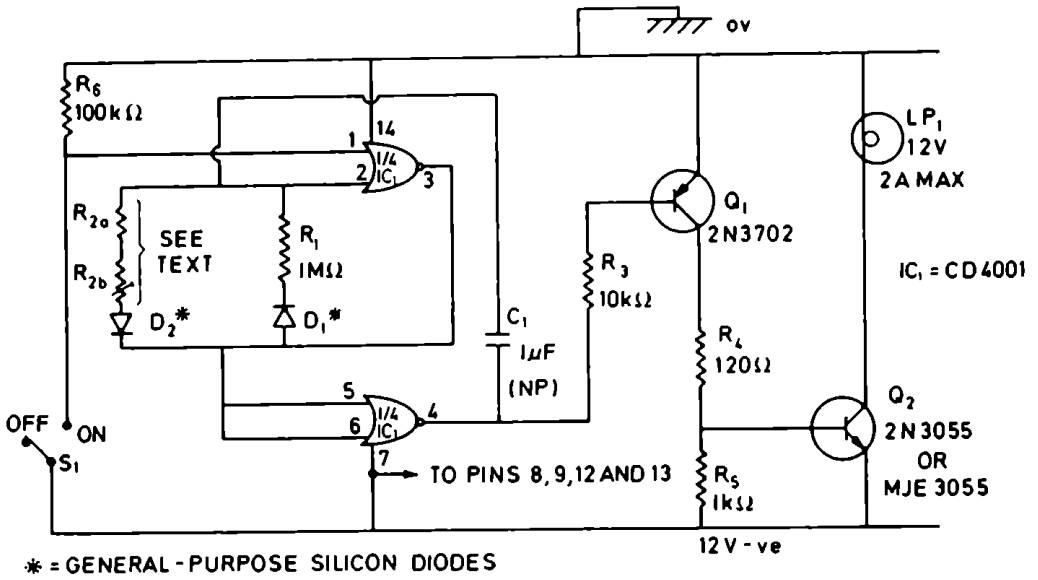


Figure 4.4 Gated and modified P-D-C lamp flasher

Figure 4.4 shows how the above circuit can be modified for use on positive-ground cars, and how ON/OFF switch S_1 can be repositioned so that it passes a gating current of only a fraction of a milliamp. The diagram also shows how R_2 can be replaced by a fixed and a variable resistor in series, so that the OFF time of the lamp is made variable. No specific values are shown for these two resistors, but it should be noted that R_{2a} determines the minimum value of the OFF time, and R_{2b} determines the maximum value.

The four lamp-flasher circuits that we have looked at so far are all activated manually. *Figures 4.5* and *4.6* show how the basic and the P–D–C circuits can be modified so that they are activated automatically when the ambient light level falls below a pre-set value. Here, a light-dependent potential divider, comprising light-dependent resistor LDR and variable resistor R_6, is wired between the circuits supply rails, and the output of the divider is taken to pin 1 of the IC, so that the potential divider gates the astable multivibrator on and off.

In practice, R_6 is adjusted so that the output of the potential divider is fractionally less than the threshold voltage of the IC at the required turn-on value of ambient light level, so that the astable is activated. Now, the resistance of the LDR is inversely proportional to

light level, and is low under bright conditions, and high under dark conditions. Consequently, if the light level falls below the pre-set value the voltage on pin 1 will fall below the threshold value, and the astable will operate. If, on the other hand, the light level rises above the pre-set value, the voltage on pin 1 will rise above the threshold value, and the astable will be disabled. Thus, the circuits turn on automatically when it gets dark, and turn off again when it gets light.

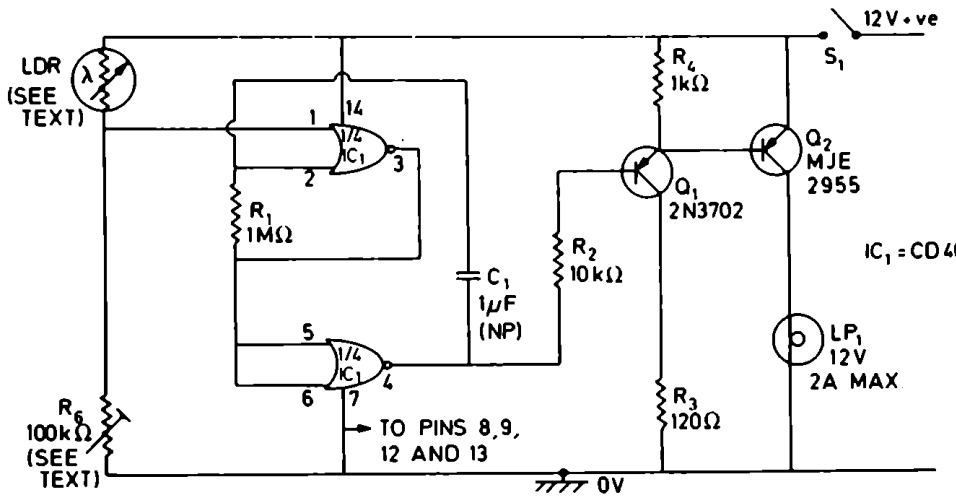


Figure 4.5 Automatic (dark-activated) d.c. lamp flasher

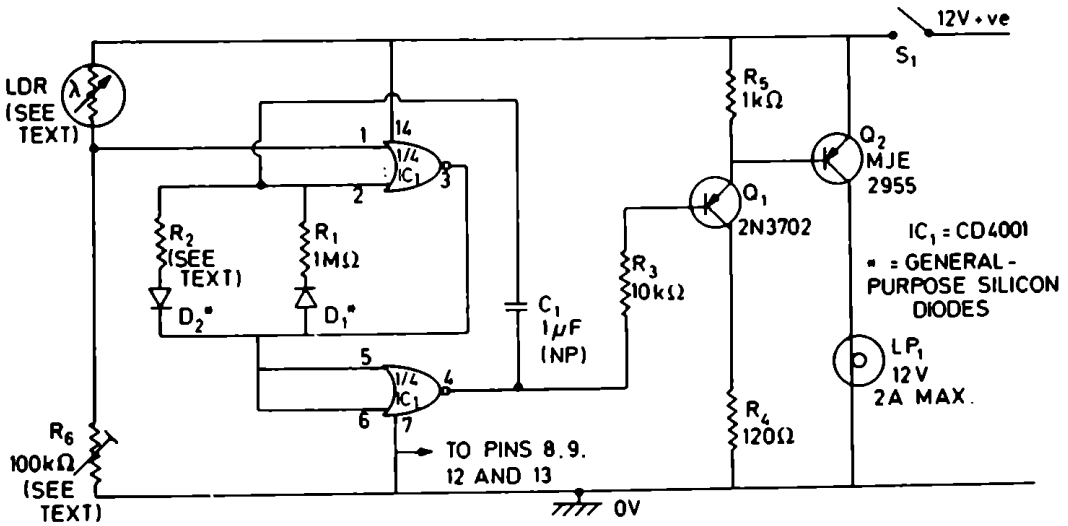


Figure 4.6 Automatic P-D-C lamp flasher

The LDRs used in these circuits can be any cadmium-sulphide photocells having resistances greater than a few thousand ohms at the required turn-on light levels. R_6 should have a maximum value that is roughly double that of the LDR under the turn-on condition. When building these circuits, note that the LDR faces must be shielded from the light of the flasher lamps, so that the circuits are sensitive to the

ambient light level but are unaffected by the lamp-flashing action. Also note that master ON/OFF switch S_1 is wired in series with the supply line of each circuit, so that each circuit can be disabled if it is put away in a dark storage area.

D. C. lamp dimmers

Figures 4.7 and *4.8* each show how one half of a CD4001 COS/MOS IC can be used in conjunction with a couple of transistors to make a d.c. lamp dimmer, in which the intensity of the lamp can be smoothly varied from zero to full brilliance via a 100 kΩ variable resistance control.

Both circuits operate in the same basic way. When S_1 is closed the astable multivibrator operates and feeds a rectangular waveform to the lamp via transistors Q_1 and Q_2. The action of the circuit is such that Q_2 is switched alternately between the fully off and the fully saturated conditions so that the power losses of the circuit are quite low. The astable operates at a fixed frequency of about 100 Hz, but its duty cycle or mark/space ratio is fully variable from approximately 1:20 to 20:1 via R_3.

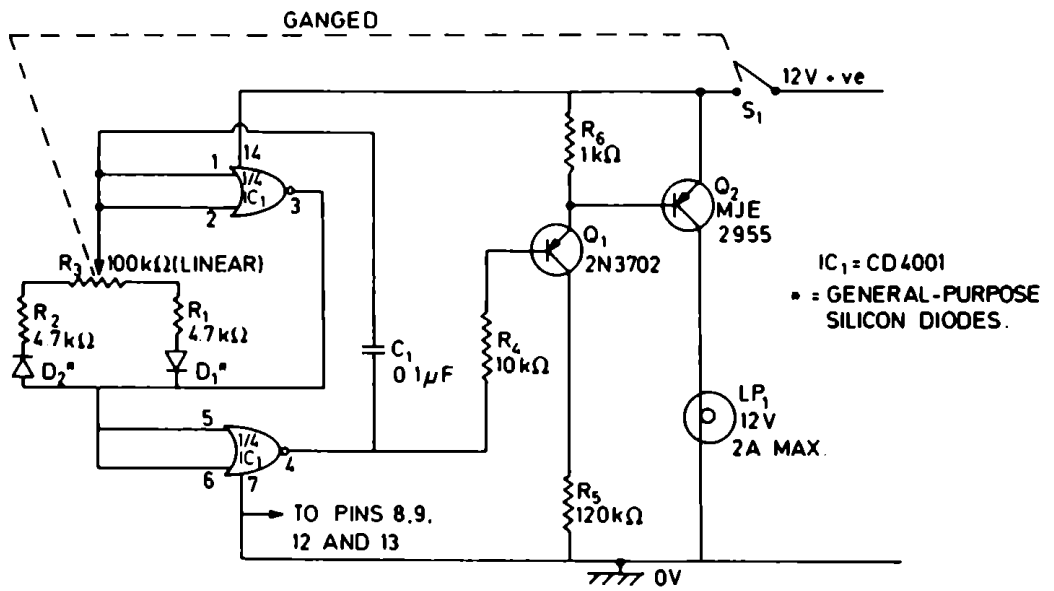


Figure 4.7 D.C. lamp dimmer, -ve ground

Consequently, the mean power to the lamp can be varied from approximately 5% to 95% of maximum via R_3. Since the period of the basic 100 Hz waveform (10 mS) is short relative to the thermal time constant of the lamp, the intensity of the lamp can be varied from

virtually zero to maximum with no sign of flicker. Note that ON/OFF switch S_1 is ganged to R_3, so that the circuit can be switched fully off by simply turning the R_3 'brilliance' control fully anticlockwise.

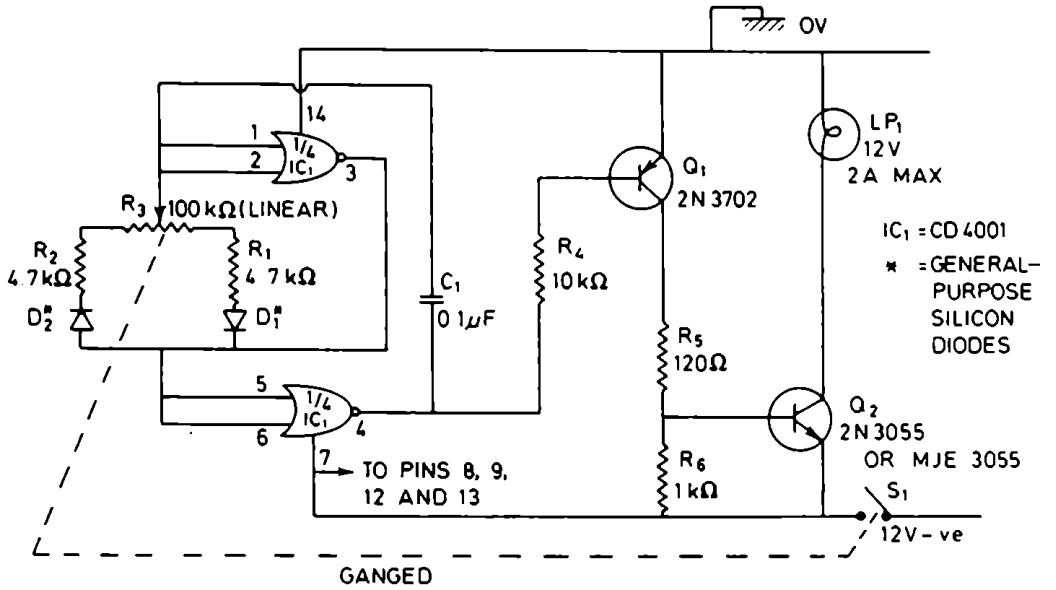


Figure 4.8 D.C. lamp dimmer, +ve ground

These lamp-dimmer circuits can be used for controlling the instrument or internal lights of cars. The *Figure 4.7* circuit is suitable for use in vehicles in which one side of the lamp goes to the negative terminal of the battery, as is common in negative ground vehicles, and the *Figure 4.8* circuit is suitable for use in cases where one side of the lamp goes to the positive terminal.

It should be noted that, although one side of each instrument and external light is invariably taken to ground (chassis) in automobiles, it is quite a common practice to take one side of the dome or courtesy light to the 'hot' side of the vehicle's battery. Great care should thus be taken in selecting the correct lamp-dimmer circuit for each specific application.

Auto-turn-off time-controlled circuits

Finally, *Figures 4.9* and *4.10* each show how one half of a CD4001 COS/MOS IC can be used in conjunction with a couple of transistors to impart an automatic-turn-off time-controlled action to a d.c. lamp. The action is such that the lamp turns on as soon as push-button switch S_1 is momentarily closed, but then turns off again automatically after a pre-set time. The time delay can be varied from a fraction of a second to several minutes.

Both circuits operate in the same basic way. Two of the gates of the IC are interconnected as a simple manually-triggered monostable multivibrator. Normally, the output of the monostable is low, so both transistors are cut off and zero power is fed to the lamp. When S_1 is

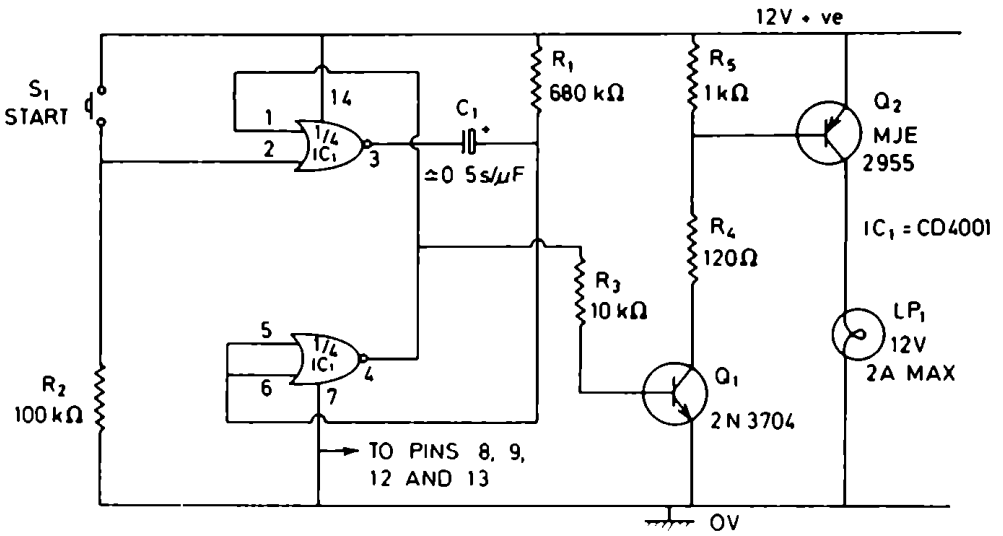


Figure 4.9 Auto-turn-off time-controlled d.c. lamp, -ve ground

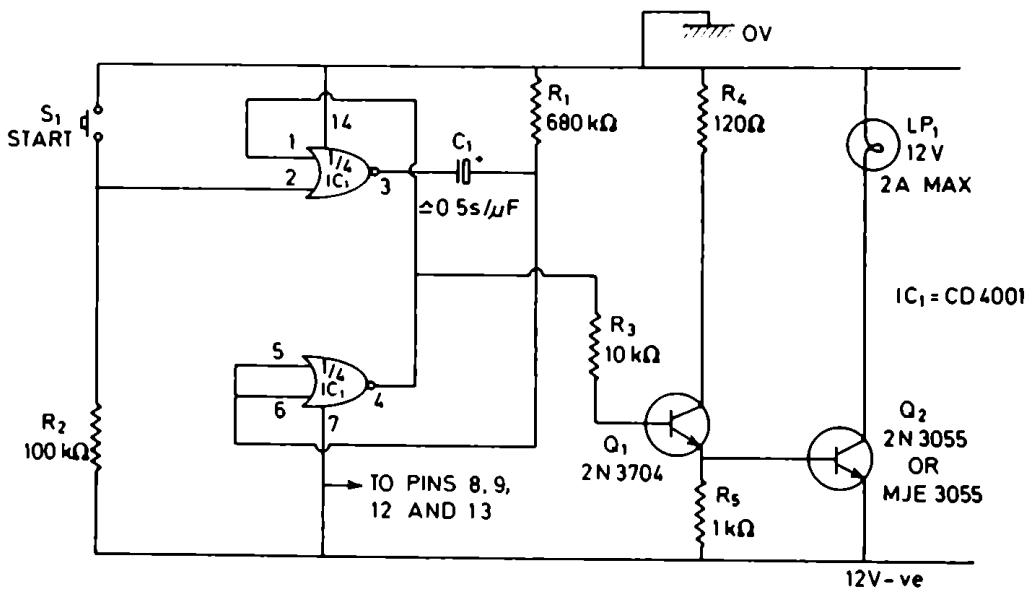


Figure 4.10 Auto-turn-off time-controlled d.c. lamp, +ve ground

momentarily closed the monostable is triggered, and its output goes high and drives both transistors and the lamp fully on. After a pre-set delay, the output of the monostable automatically switches back to the low state again, and the transistors and the lamp turn off. The circuit action is then complete.

The time delay of each circuit is determined by the value of R_1 and C_1, and approximately equals 0.5 s/μF of C_1 value when R_1 has the value of 680 kΩ shown. C_1 can be an electrolytic component, and can have any value up to a maximum of 1000 μF or so, thus giving periods up to several minutes. This capacitor must, however, have reasonably low leakage characteristics.

The two circuits are suitable for controlling the external lights of cars, etc., and the *Figure 4.9* circuit is intended for use on negative-ground vehicles, and the *Figure 4.10* circuit is for use in positive-ground vehicles.

CHAPTER 5

20 RELAY-SWITCHING CIRCUITS

COS/MOS digital ICs can readily be used to provide a variety of useful relay-switching functions. In the present chapter we show 20 different ways of using COS/MOS to make high-impedance relay switches, semi-precision voltage-activated relay switches, heat and light-activated relay switches, time-delayed relay switches, and miscellaneous devices such as relay pulsers and water-activated relay switches. All of the circuits shown are designed around the ubiquitous CD4001 quad 2-input NOR gate, and are intended for 12 V operation using relays with coil resistances of 180 Ω or greater.

High-impedance relay switches

Figure 5.1 shows how one of the gates of a CD4001 IC can be used in conjunction with a single transistor to make a simple high-impedance relay switch. The operation of the circuit is quite simple. The COS/MOS gate is connected as a simple inverter, with its input tied to the OV rail via 10 MΩ resistor R_1, and with its output taken to the relay via pnp transistor Q_1.

Normally, with zero input applied, the output of the COS/MOS gate is at full positive-rail potential, so that zero bias is applied to Q_1 via R_2, and Q_1 and the relay are off. The circuit consumes a typical standby or leakage current of about 1 μA under this condition. When, on the other hand, an input voltage greater than the threshold value of the IC is applied to the circuit, the output of the gate drops to virtually OV, and under this condition Q_1 is biased fully on via R_2, and the relay turns on.

The input impedance of the above circuit is equal to the R_1 value, and equals 10 MΩ with the component value shown. The relay in the above circuit actually turns on or off when the input voltage approximates the threshold value of the IC, and under this condition the IC is biased into its linear amplifying state. C_1 is used to inhibit any high frequency or transient instability that might occur in the IC under this specific condition. In practice, the relay turns on when the input voltage approximates half of the supply voltage.

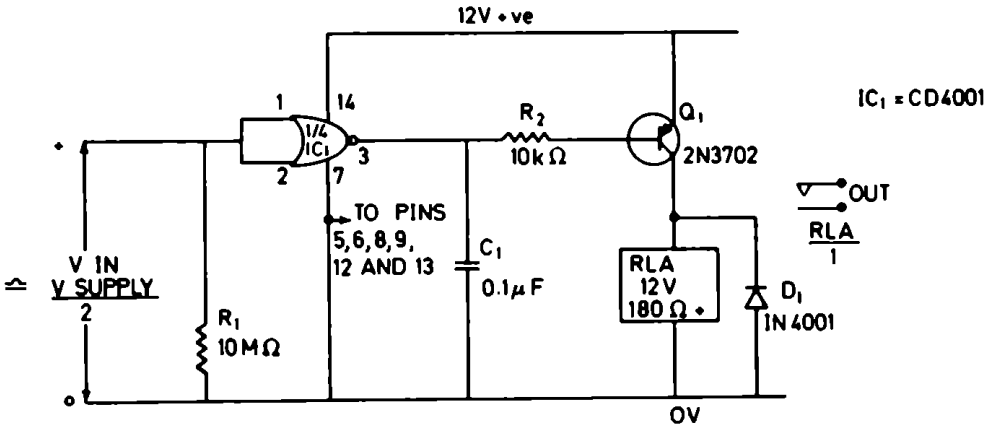


Figure 5.1 Simple high-impedance relay switch

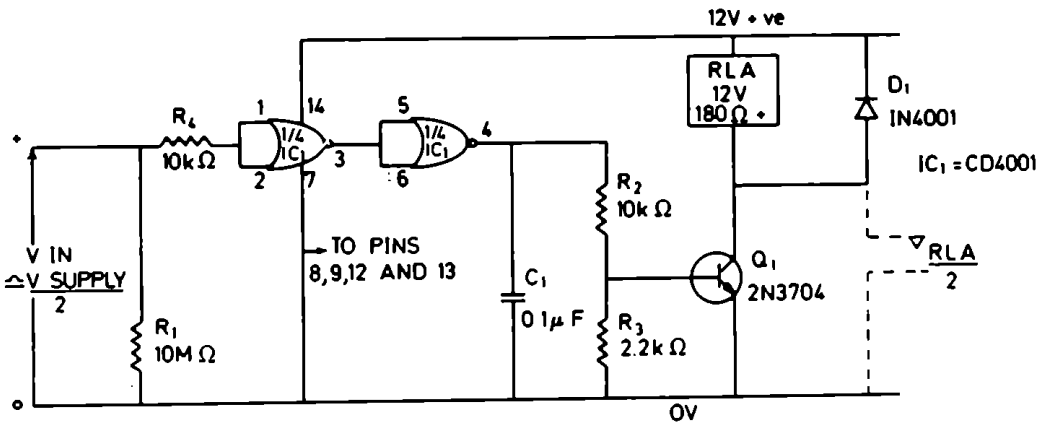


Figure 5.2 Modified high-impedance relay switch

The performance of the simple *Figure 5.1* high-impedance circuit can be improved or modified in a number of ways. *Figure 5.2*, for example, shows how the output of the gate can be taken to the relay via a second COS/MOS inverter stage and via an npn transistor. This modification causes the turn-on and turn-off input voltages of the relay switching circuit to be more sharply defined, and causes the 'backlash' of the circuit to be greatly reduced. The performance of the circuit is also enhanced by wiring R_3 between the base and emitter of Q_1, so

that Q_1 begins to turn on when the voltage of C_1 rises to approximately 3.6 V, rather than to only 0.6 V as in the case of the simpler circuit. C_1 is again used to enhance circuit stability. R_4 is an input-protection 'safety' resistor.

The *Figure 5.2* circuit can be made self-latching, if required, by simply wiring a spare set of normally-open relay contacts between the collector and emitter of Q_1, as shown dotted in the diagram. Alternatively, if a spare set of relay contacts are not available, a self-latching high-impedance relay switch can be made by using the connections shown in *Figure 5.3*.

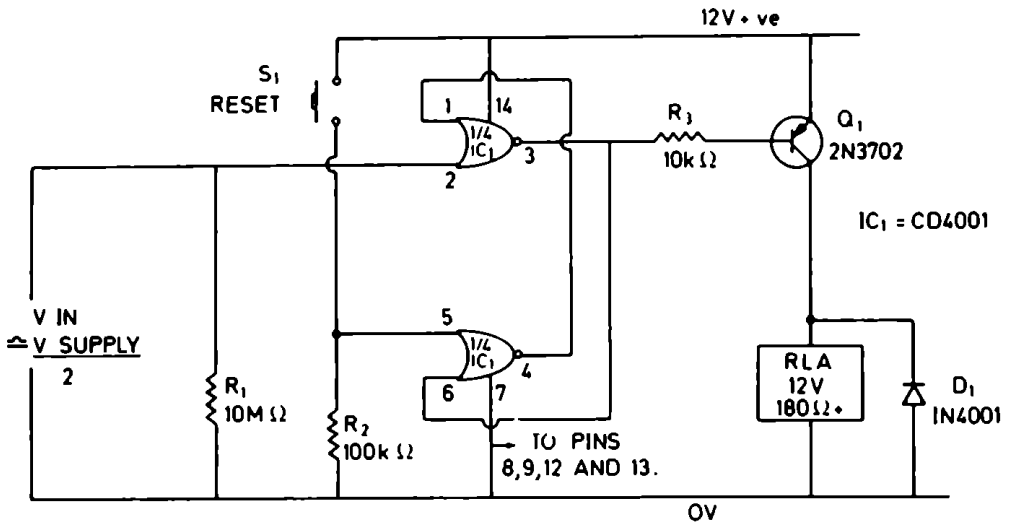


Figure 5.3 Self-latching high-impedance relay switch

Here, a pair of COS/MOS 2-input NOR gates are cross-coupled to form a simple bistable multivibrator, and the output of the bistable is taken to the relay via Q_1. The relay can be turned on and made to self-latch by feeding a suitable voltage level to the circuit's input terminal. Once the relay has turned on and self-latched, it can be turned off again by simply removing the input voltage and briefly closing RESET switch S_1. The input impedance of the circuit is equal to the R_1 value, and is 10 MΩ in this particular case.

Finally, *Figure 5.4* shows the connections for making a 4-input high-impedance relay switch, in which the relay can be activated via any one of four independent high-impedance input terminals, each with an impedance of 10 MΩ.

Here, two of the CD4001 gates are connected as NOR elements, and have their outputs taken to the relay via diodes D_1 or D_2 and transistor Q_1. Normally, with all inputs at zero, the outputs of both gates are high, so zero base drive is applied to Q_1, andQ_1 and the relay are off. When, on the other hand, a suitable positive input is applied to any one

of the circuit's input terminals, the output of one or other of the two gates is driven to OV. Under this condition base drive is applied to Q_1 via R_5 and D_1 or D_2, and the transistor and the relay turn on. The relay can thus be activated via any one of the four input terminals.

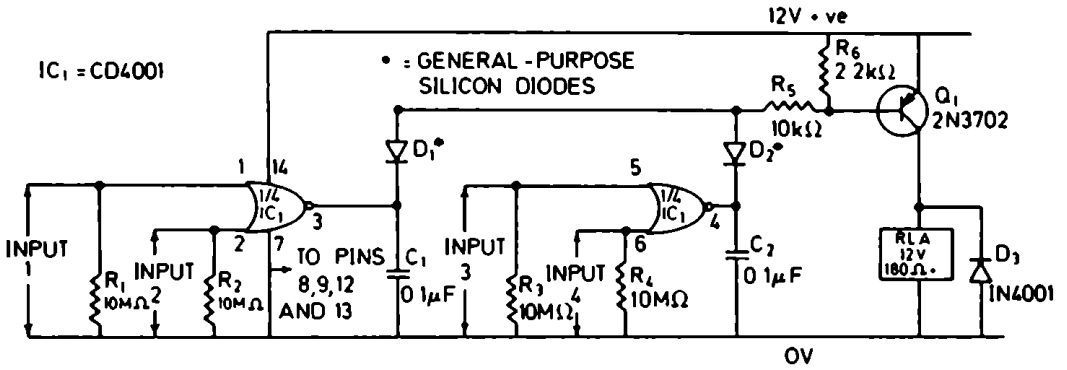


Figure 5.4 4-input high-impedance relay switch

The *Figure 5.4* circuit utilises only two of the available gates of the CD4001 IC. If required, the circuit can be expanded to accommodate 8-input activation by simply utilising all four of the available gates of the CD4001 IC.

Semi-precision voltage-activated relay switches

The turn-on voltage of the high-impedance relay switching circuit of *Figure 5.2* is quite sharply defined, and is determined by the threshold voltage value of the individual COS/MOS IC that is used, and by the

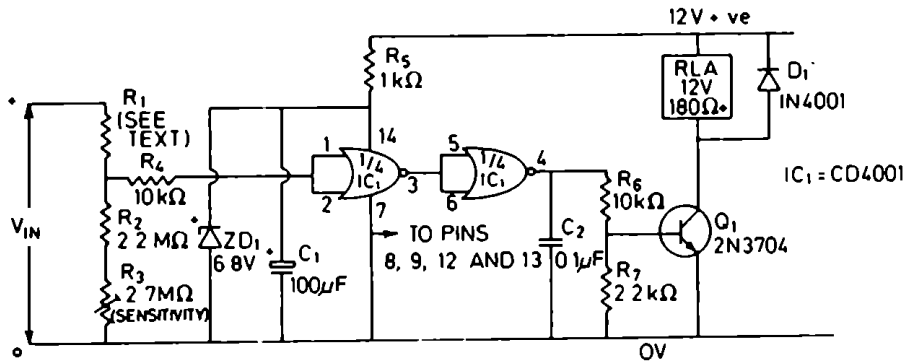


Figure 5.5 Semi-precision over-voltage relay switch

value of supply voltage that is employed. The 'backlash' of the circuit is very low, and thus the turn-on and turn-off voltages of the design are almost identical.

The threshold voltage of a COS/MOS IC is almost independent of normal changes in ambient temperature, so the precision of the turn-on voltage of the *Figure 5.2* circuit is determined primarily by the precision of its supply voltage regulation. Consequently, the *Figure 5.2* circuit can be made to function as a semi-precision voltage-activated relay switch by simply stabilising the supply voltage of its COS/MOS stages as shown in the circuit of *Figure 5.5.*

The *Figure 5.5* circuit is identical to that of *Figure 5.2*, except that its COS/MOS supply rail is stabilised at 6.8 V by R_5–C_1 and zener diode ZD_1, and its input is applied via potential divider R_1–R_2–R_3 and via safety resistor R_4. The circuit is designed so that the relay turns on only when the input voltage exceeds a pre-set value. If required, the circuit can be modified so that the relay turns on only when the input voltage falls below a pre-set value by simply interposing a spare COS/MOS inverter stage between pin 4 of the IC and the input of the transistor stage, as shown in *Figure 5.6*.

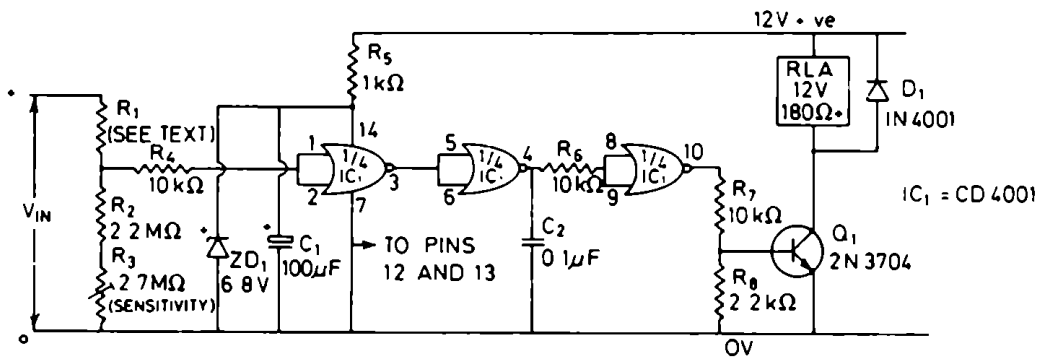


Figure 5.6 Semi-precision under-voltage relay switch

The *Figures 5.5* and *5.6* circuits both have basic input sensitivities of 1 MΩ/V, and are intended to be used with input voltages that are greater than the nominal 3.4 V threshold voltages of the COS/MOS ICs that are used. Range resistor R_1 is selected on the basis of 1 MΩ/V–3.4 MΩ. Thus, for a 10 V input R_1 is given a value of approximately 6.6 MΩ (in practice, 6.8 MΩ). Pre-set resistor R_3 enables the sensitivity of the circuit to be adjusted over a limited range, to compensate for variations in the threshold voltages of individual COS/MOS ICs, and to enable standard-value range resistors to be selected. The two circuits have typical voltage-switching accuracies of about 1%.

Time-delayed relay switches

The CD4001 COS/MOS IC can be used in a number of simple but effective time-delayed relay switching applications. *Figure 5.7*, for

example, shows how one of the gates of this IC can be used to give a delayed turn-on relay switching action, with delays ranging from a fraction of a second up to several minutes.

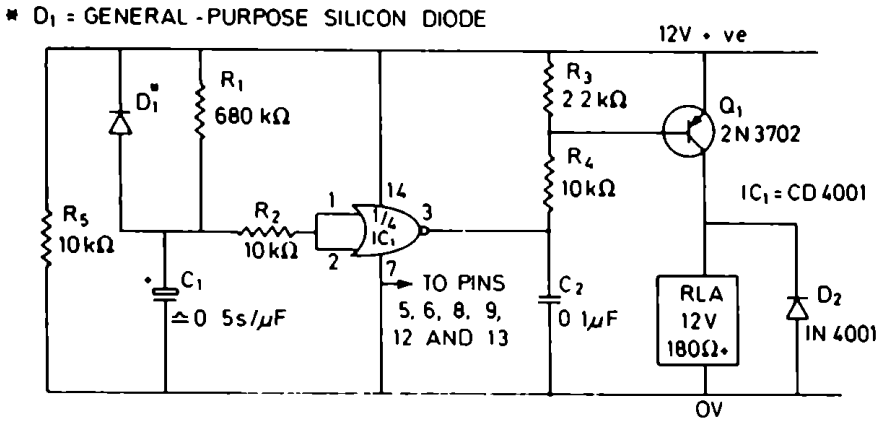


Figure 5.7 Delayed-turn-on relay switch

Here, the COS/MOS gate is wired as a simple pulse inverter, with its output feeding to the relay via pnp transistor Q_1, and with its input taken from the junction of the time-controlled potential divider formed by R_1 and C_1. The operation of the circuit is quite simple.

When power is first applied to the circuit, C_1 is fully discharged, and thus the input of the inverter is effectively grounded and its output is at full positive-rail potential. Under this condition zero base drive is applied to Q_1, so that Q_1 and the relay are off. As soon as the power is applied to the circuit, C_1 starts to charge up via R_1, and a rising exponential

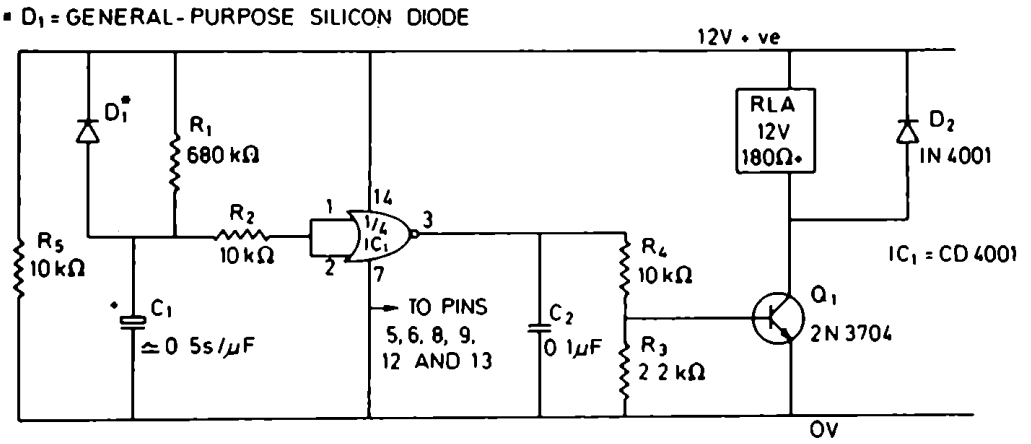


Figure 5.8 Auto-turn-off relay switch

voltage is applied to the input of the inverter stage. After a delay determined by the C_1 and R_1 values, this voltage rises above the threshold value of the COS/MOS inverter stage, and its output swings towards the OV rail and drives Q_1 and the relay on via R_4. The relay then remains

on until power is removed from the circuit, at which point C_1 discharges rapidly via D_1 and R_5. The operating sequence is then complete.

If required, the operation of the above circuit can be reversed, so that the relay turns on as soon as power is applied but then turns off again automatically after a pre-set delay, by simply modifying the relay-driving transistor stage for npn operation, as shown in *Figure 5.8.* In either case, the circuits both give a time delay of approximately 0.5s/μF of C_1 value, thus enabling delays up to several minutes to be obtained. If required, the delay periods can be made variable by replacing R_1 with a fixed and a variable resistor in series.

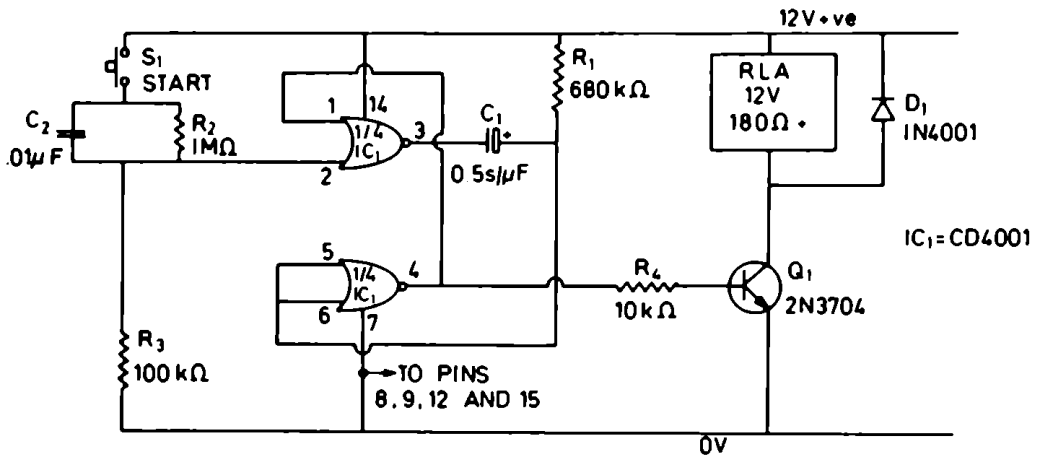


Figure 5.9 One-shot relay time switch

Finally, *Figure 5.9* shows the connections for making a push-button-activated one-shot relay switch that gives time delays up to several minutes. The action is such that the relay turns on as soon as START switch S_1 is momentarily closed, but turns off again automatically after a pre-set delay. The delay is roughly equal to 0.5s/μF of C_1 value. As can be seen, the circuit simply consists of a manually-triggered one-shot or monostable multivibrator, as described in Chapter 3, with its output feeding to the relay via R_4 and Q_1.

Temperature-activated relay switches

The CD4001 quad 2-input NOR gate IC can readily be used to make a variety of heat and light-activated relay switching circuits. *Figure 5.10,* for example, shows a very simple way of using the IC to make an under-temperature relay switch, which turns on when the temperature falls below a pre-set level.

Here, one of the COS/MOS gates is connected as a simple inverter, and its output is taken to the relay via Q_1. The input of the inverter is

taken from the junction of the temperature-sensitive potential divider formed by R_1 and TH_1. TH_1 is an inexpensive negative-temperature-coefficient thermistor. The resistance of this thermistor is inversely proportional to temperature, and is high at low temperatures and low at high temperatures. Consequently, the voltage of the R_1-TH_1 junction rises as the temperature falls.

In practice, R_1 is adjusted so that the voltage at the R_1-TH_1 junction equals the threshold voltage of the COS/MOS gate, and the relay just turns on at the required switching temperature. Thus, at temperatures above this level the voltage is below the threshold value, and the relay is off, while at temperatures below this level the voltage is above the threshold value, and the relay is on. This simple circuit has a typical temperature switching accuracy of better than 1°C.

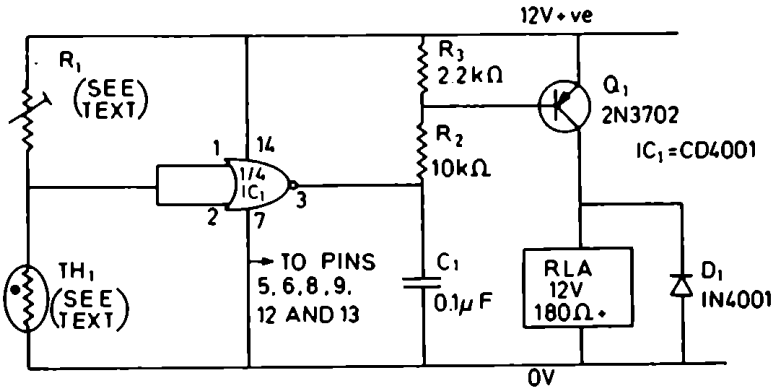


Figure 5.10 Under-temperature relay switch

The action of the above circuit can be reversed, so that the relay turns on when the temperature goes above a pre-set level, by simply transposing the R_1 and TH_1 positions, as shown in the over-temperature relay switching circuit of *Figure 5.11.*

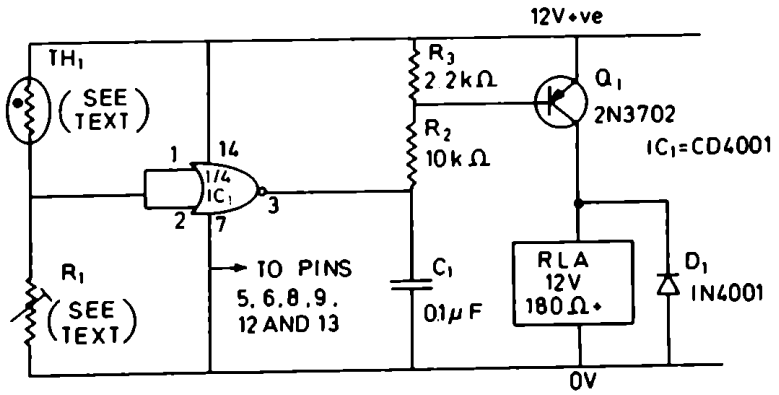


Figure 5.11 Over-temperature relay switch

The thermistors used in these and all other temperature-activated circuits shown in the chapter can be any negative-temperature-coefficient devices that have resistances in the range 2 kΩ to 2 MΩ at

the required turn-on temperature levels. The variable resistor associated with the thermistor (R_1 in *Figures 5.10* and *5.11*) should have a maximum value that is roughly double that of the thermistor at the required switching level, so that the potential divider can be set to give half-supply voltage with the variable resistor at its half-value setting.

The circuits of *Figures 5.10* and *5.11* each use only one quarter of the number of available gates of a CD4001 IC. If required, the two circuits can be built from a single IC, as shown in *Figure 5.12*, to form a dual-output temperature-deviation switch in which *RLA* goes on when the temperature goes above a pre-set level and *RLB* goes on when the temperature falls below a pre-set level.

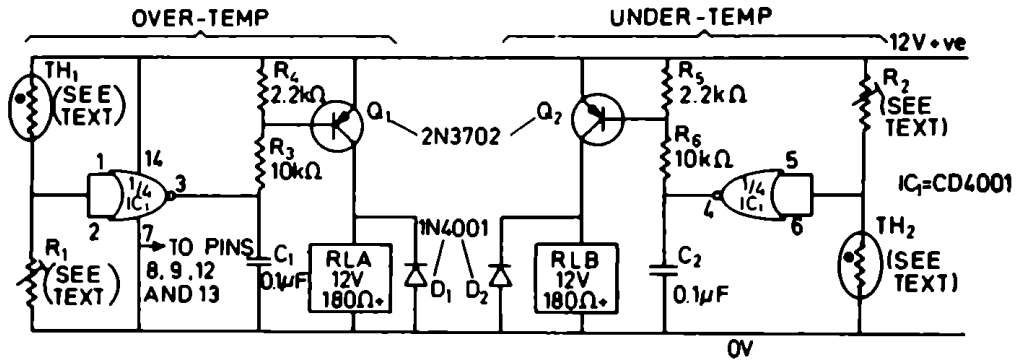


Figure 5.12 Dual-output temperature deviation switch

Alternatively, the circuits can be combined and modified to form a single-output temperature-deviation switch, in which a single relay turns on when the temperature goes above or below pre-set levels, by using the connections shown in *Figure 5.13.*

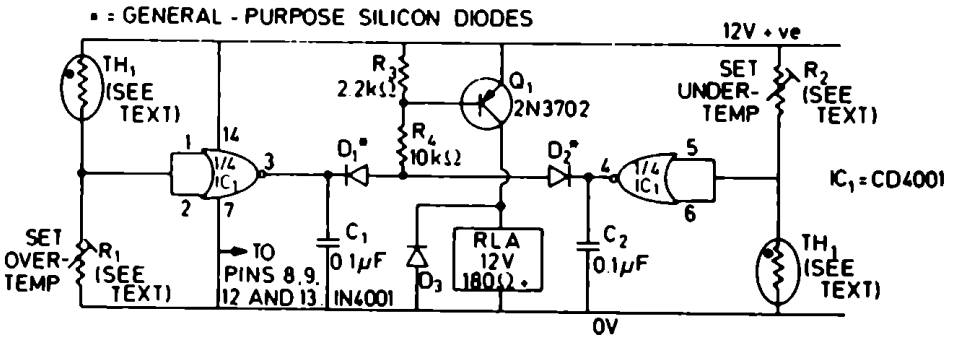


Figure 5.13 Single-output temperature-deviation switch

Here, the transistor and relay are driven on via D_1 if the temperature exceeds a value that is pre-set via R_1, and are driven on via D_2 if the temperature falls below a value pre-set via R_2. The two temperature-switching circuits are quite independent of each other, and so there is no interaction of the two temperature-switching levels.

Finally, *Figure 5.14* shows the circuit of a temperature-activated relay pulser, in which the relay starts to pulse on and off at a pre-set rate when the temperature exceeds a pre-set level. The pulse rate is variable from approximately 26 to 80 pulses per minute via R_3.

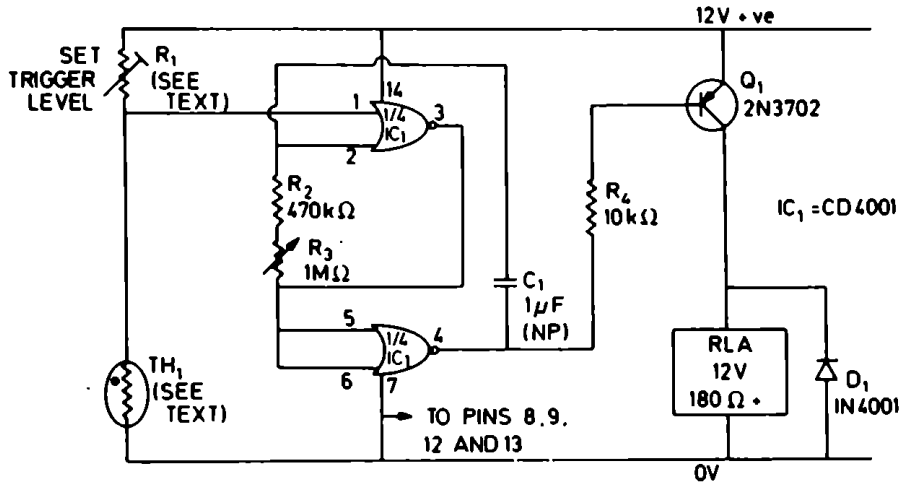


Figure 5.14 Temperature-activated relay pulser

The circuit is simply a gated astable multivibrator, of the type described in Chapter 3, with its output taken to the relay via Q_1, and its gate input derived from the output of the temperature-sensitive potential divider formed by R_1 and TH_1. The circuit can be used to flash a lamp or operate an alarm bell or buzzer when the temperature exceeds a pre-set level.

The operation of the *Figure 5.14* circuit can be reversed, so that the relay activates when the temperature falls below a pre-set level, by simply transposing the R_1 and TH_1 positions.

Light-activated relay switches

The temperature-activated relay switching circuits of *Figures 5.10* to *5.14* can be modified for light-activation by simply replacing their temperature-sensitive potential dividers with light-sensitive units. *Figure 5.15*, for example, shows how the over-temperature switching circuit of *Figure 5.11* can be converted to a simple light-operated relay switch by using a light-dependent resistor (LDR) in place of the thermistor.

The LDR used in this and all other circuits shown in the chapter can be any cadmium-sulphide photocell that has a resistance in the range 2 kΩ to 2 MΩ at the required light switching level. The variable resistor

associated with the LDR (R_1 in *Figure 5.15*) should have a maximum value that is roughly double that of the LDR at the required switching level, so that the potential divider can be set to give half-supply voltage with the variable resistor at its half-value setting.

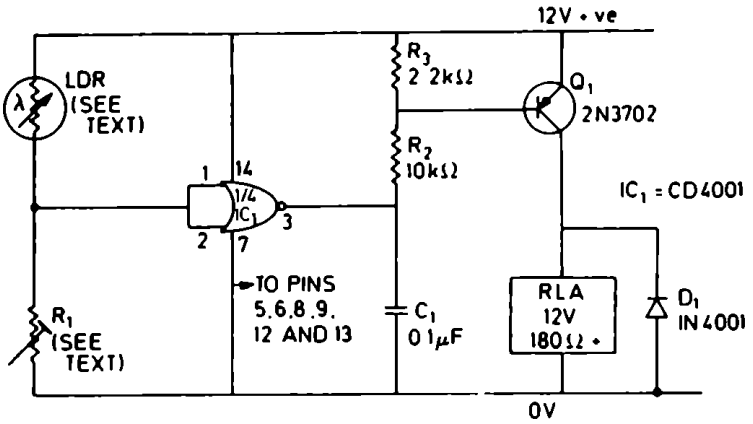


Figure 5.15 Simple light-operated relay switch

Cadmium-sulphide photocells develop a low resistance under bright conditions, and a high resistance under dark conditions. Consequently, under bright conditions a high voltage is fed to the input of the COS/MOS gate of the *Figure 5.15* circuit, and the relay is driven on, but under dark conditions a low voltage is applied to the gate, so the relay is off.

The action of the above circuit can be reversed, so that the relay goes on when the light intensity falls below a pre-set level, by simply transposing the R_1 and LDR positions, as shown in *Figure 5.16*. This

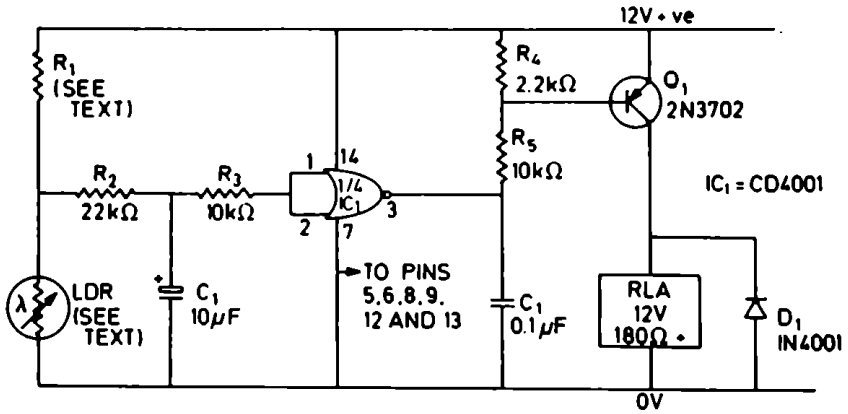


Figure 5.16 Dark-operated relay switch, with transient suppression

circuit also shows how a simple transient-suppressing smoothing network can be wired between the output of the light-sensitive potential divider and the input of the COS/MOS gate, so that the circuit is

sensitive to mean light levels, but is unaffected by sudden transient changes in light level (such as are caused by lightening flashes, etc). This circuit can be used to automatically turn the parking lights of a car or the porch lights of a house on at dusk and off at dawn.

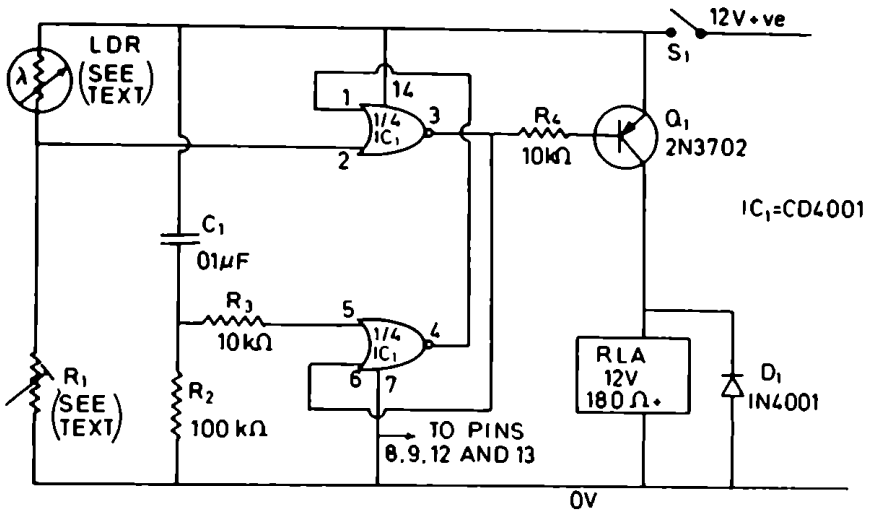


Figure 5.17 Self-latching light-operated relay switch

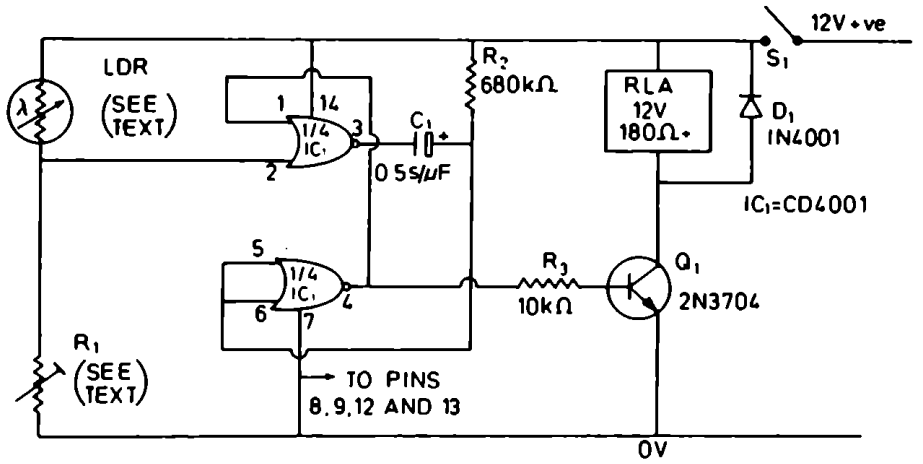


Figure 5.18 Light-activated one-shot relay switch

Figure 5.17 shows the connections for making a self-latching light-operated relay switch, which turns on when the light level exceeds a pre-set value, but can be turned off again only by breaking the supply connections via switch S_1. The circuit consists of a simple bistable multivibrator, with its output taken to the relay via Q_1, and its trigger input taken from the R_1–*LDR* junction of the light-sensitive potential divider. Pin 5 of the IC is taken to the positive supply rail via R_3 and C_1, so that a 'reset' pulse is automatically applied to the circuit at the moment that the supply is connected via S_1.

This circuit can be usefully employed to sound an alarm if a safe door is opened without authority. In this application the LDR must be placed inside the safe, and the remaining circuitry can be placed externally, with S_1 taking the form of a normally-closed key-operated switch. Thus, if the safe is opened by an unauthorised person light will fall on the LDR face and cause the alarm to operate and self-latch, however, an authorised person can disable the alarm via key-switch S_1 prior to opening the safe door, and thus gain access with immunity.

If required, the action of the above circuit can be modified, so that the relay turns off automatically, after a pre-set period, by using a monostable or one-shot multivibrator in place of the bistable multivibrator, as shown in *Figure 5.18*. This circuit gives delays of approximately 0.5 s/μF of C_1 value, and can be made to give delays of several minutes by using high-value capacitors.

Miscellaneous relay-switching circuits

Finally, to conclude this chapter, *Figures 5.19* and *5.20* show two simple but useful relay-switching circuits of miscellaneous types. The *Figure 5.19* circuit is that of a relay pulser, which causes the relay to pulse on and off at a rate variable between approximately 26 and 80 pulses per minute when S_1 is closed. The rate is variable via R_2. This circuit can be used as an emergency lamp flasher, etc., by using the relay contacts to switch power to the lamps.

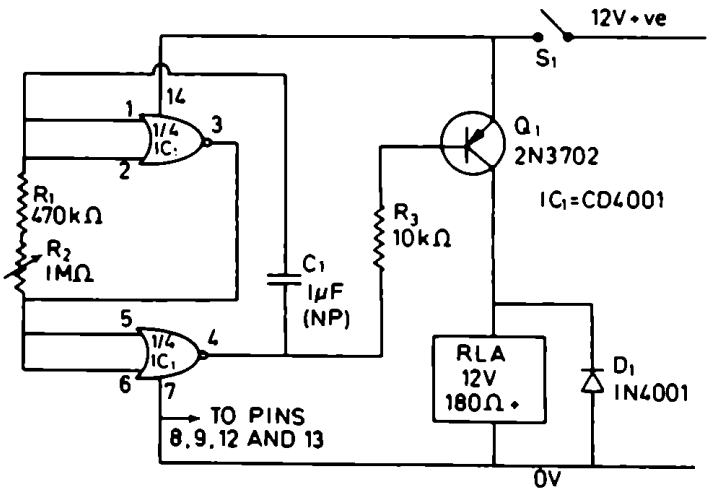


Figure 5.19 Relay pulser (Rate ≃ 26 to 80 pulses per minute)

The *Figure 5.20* circuit is that of a water-activated relay switch. The operation of the circuit is very simple. Water has a relatively low

resistivity. Consequently, when the two probes are placed in water (or some other conductive liquid), the potential divider action of R_1 and the liquid resistance causes a high voltage to be applied to the input of

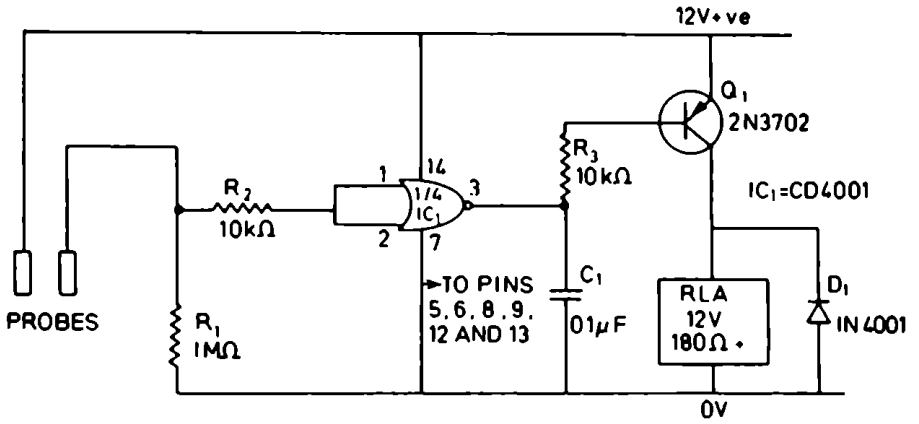


Figure 5.20 Water-activated relay switch

the COS/MOS gate, and the relay is driven on. When the probes are not in a conductive liquid, the input of the COS/MOS gate is effectively grounded via R_1, and the relay is off. This circuit can be used to sound an alarm when water reaches a pre-set level in a tank, bath, or other container.

CHAPTER 6

25 SOUND GENERATOR AND ALARM CIRCUITS

The CD4001 quad 2-input NOR gate can be readily used in a variety of sound generator and electronic alarm applications. In the present chapter we show 25 ways of using this IC in applications of these types. The circuits shown range from miscellaneous sound generators such as code-practice oscillators and electronic metronomes, to pulsed-output alarm generators that can be activated by exposure to heat or light, or by contact with water. Included among the circuits are a number of basic alarm-generator designs, and a variety of burglar alarm systems.

Miscellaneous sound-generator circuits

Figure 6.1 shows how a CD4001 IC can be used in conjunction with a single transistor to make a simple audible-output continuity tester. The circuit delivers maximum audible output when the test contacts have near-zero resistance, and gives a very low or zero output if the contacts have a resistance greater than a few hundred ohms.

The circuit is quite simple. Two of the gates of the IC are cross-coupled to form an 800 Hz astable multivibrator or square-wave generator. The output of the astable is fed to the speaker via R_2, Q_1, and R_X. The combined series resistance value of the speaker and R_X is approximately 100 Ω, (to ensure that the power rating of Q_1 is not exceeded under operating conditions), and the speaker can have any impedance in the range 3 Ω to 100 Ω. The test contacts are connected in series with the circuit's positive supply line via a pair of probes.

Thus, if the contacts have zero resistance the full supply voltage is connected to the circuit, and a fairly high sound level is generated by

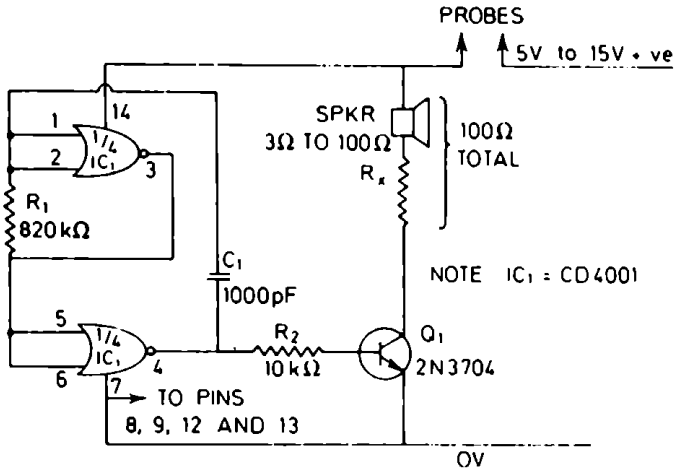


Figure 6.1 Continuity tester

the speaker. If the contacts have a resistance of 100 Ω the sound output falls to about half of its maximum value, and if the resistance is 1 kΩ the sound output falls to about one-tenth of maximum. The circuit can be used with any supply voltage in the range 5V to 15V.

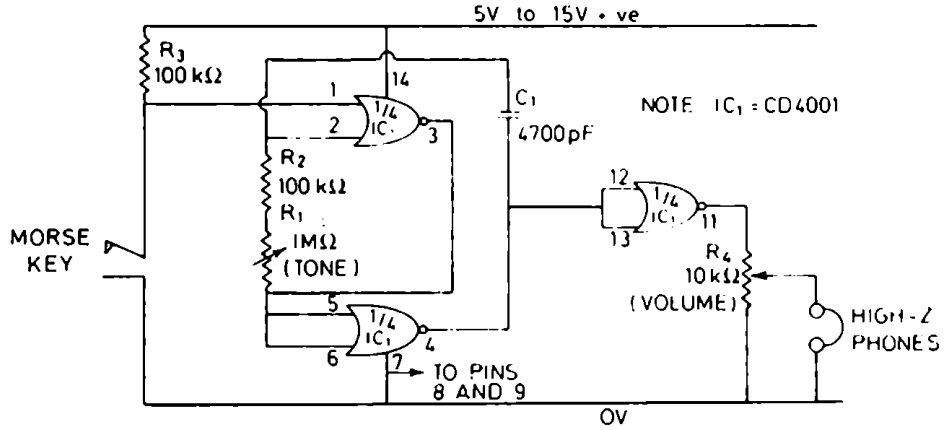


Figure 6.2 Code-practice oscillator

Figure 6.2 shows the circuit of a simple but very efficient code-practice oscillator. Here, two of the gates of the IC are connected as a gated astable multivibrator, with its input derived from the morse key, and its output taken to a pair of high-impedance phones via R_4 and one of the spare gates of the IC. The tone of the circuit can be varied between approximately 300 Hz and 3 kHz via R_1, and the 'phone volume is variable via R_4.

Normally, with the morse key open, the astable is biased off via R_3, and no tone is generated in the 'phones. The circuit draws a typical

standby current of only 0.003 μA under this condition, so that the design can be permanently connected to its supply batteries without need of a separate ON/OFF switch. When the morse key is closed the astable multivibrator is gated on, and under this condition a tone is generated in the 'phones. The 'phones can have any impedance greater than a few hundred ohms, and the circuit can be used with any supply in the range 5 V to 15 V.

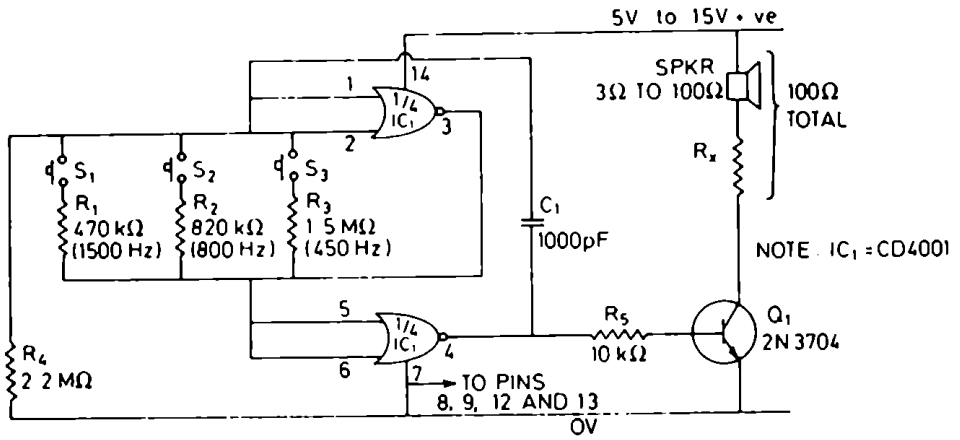


Figure 6.3 Door announcer

Figure 6.3 shows the circuit of a low-power 'door announcer'. The circuit is provided with three tone-selecting push buttons, each located in a different part of the house. Thus, when a person presses one of the buttons, their location is evident from the tone that is generated in the speaker. The three tones are each spaced approximately one octave apart so that each button generates a very distinctive note.

The circuit uses two of the gates of a CD4001 IC. Normally, with all three tone-selecting S_1 to S_3 switches open circuit, the two gates are simply connected as cascaded inverters, with the input of the upper gate tied to ground via R_4. Under this condition the circuit is inactive, and consumes a typical standby current of about 1 μA (= the leakage current of Q_1).

When any one of the tone-selecting S_1 to S_3 push-button switches are closed, the gates are connected as a simple astable multivibrator, and the circuit oscillates at a frequency determined by tone-selecting resistors R_1 to R_3. The output of the astable is taken to the speaker via $R_5 - Q_1$ and R_X so that a definite tone is generated in the speaker under this condition. Note that, for satisfactory operation, R_4 must have a value that is substantially greater than the largest of the tone-selecting resistors.

As in the case of the *Figure 6.1* circuit, the sum of the speaker resistance and R_X in *Figure 6.3* must be approximately 100 Ω, and the

circuit can be used with any supply in the range 5V to 15V. The available acoustic output power of the circuit depends on the value of supply voltage used, and on the impedance of the speaker. Using a 9V supply the mean output current is fixed at about 40 mA, so that the output power to a 15 Ω speaker is about 25 mW, and to a 100 Ω speaker about 160 mW.

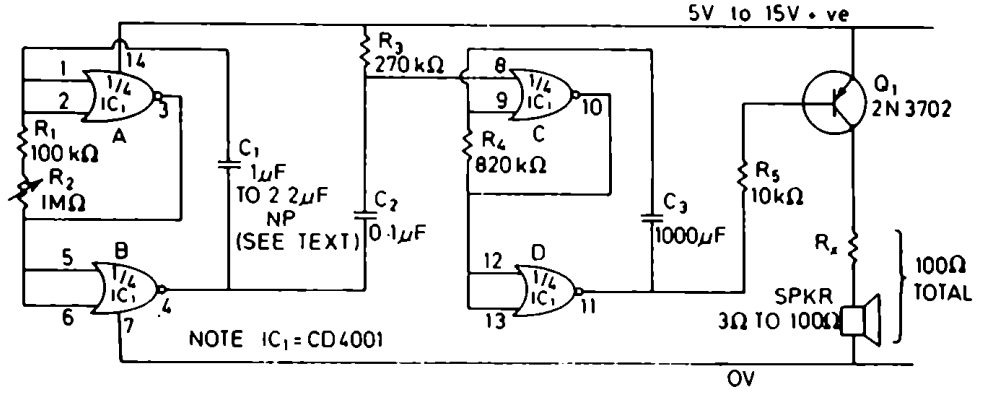


Figure 6.4 Musician's metronome

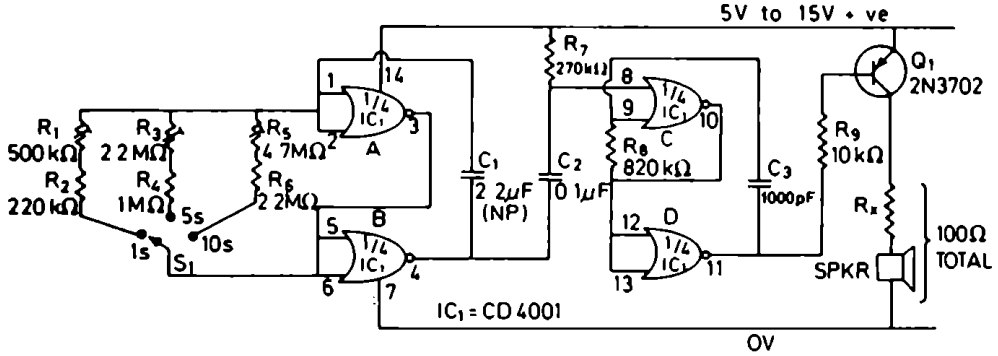


Figure 6.5 Photographic metronome

Finally, to complete this section of the chapter, *Figures 6.4* and *6.5* show two electronic metronome circuits. The *Figure 6.4* circuit is that of a musician's metronome, which covers the range 30 to 300 beats per minute, and thus encompasses the usual musical tempo range of largo (40 beats per minute) to presto (250 beats per minute). The *Figure 6.5* circuit is that of a photographic metronome, which generates a metallic 'tick' output pulse of tone at pre-set periods of 1, 5, and 10 seconds. The *Figure 6.4* circuit operates as follows.

Gates A and B of the IC are connected as a simple astable multivibrator or square-wave generator, with its frequency variable between approximately 0.5 Hz (30 cycles per minute) and 5 Hz (300 cycles per minute) via R_2. Gates C and D are connected as a gated 800 Hz astable multivibrator, with its output feeding to the speaker via R_5–Q_1 and

R_X. The output of the A–B astable is fed to the input of the C–D astable via R_3 and C_2, which differentiate the negative-going output steps of the A–B oscillator and drive the C–D multivibrator on for approximately 20 mS periods each time that the A–B astable completes a cycle.

Thus, 20 mS pulses of 800 Hz tone are generated in the speaker at rates variable (via R_2) between 30 and 300 pulses or beats per minute. These pulsed tones have a metallic 'tick' sound, and give an acceptable representation of the sound of a mechanical metronome.

To set up the *Figure 6.4* circuit, set R_2 to its maximum resistance and then adjust the value of non-polarised capacitor C_1 to produce approximately 30 beats per minute in the speaker. The rate will then rise to approximately 300 beats per minute when the R_2 value is reduced to zero. The R_2 scale can be calibrated in beats per minute using a stop-watch or other time-piece.

The photographic metronome circuit of *Figure 6.4* works in the same basic way as the circuit described above, except that the output pulses are selected via S_1 at pre-set rates of 1, 5, and 10 seconds. These periods can be precisely pre-set via R_1, R_3, and R_5 respectively. The circuit is specifically intended to give its owner an audible indication of the passage of time when working under darkroom conditions.

Basic alarm-generator circuits

The CD4001 IC can be used, in conjunction with one or more transistors, in a variety of alarm-call generator applications. *Figure 6.6*, for

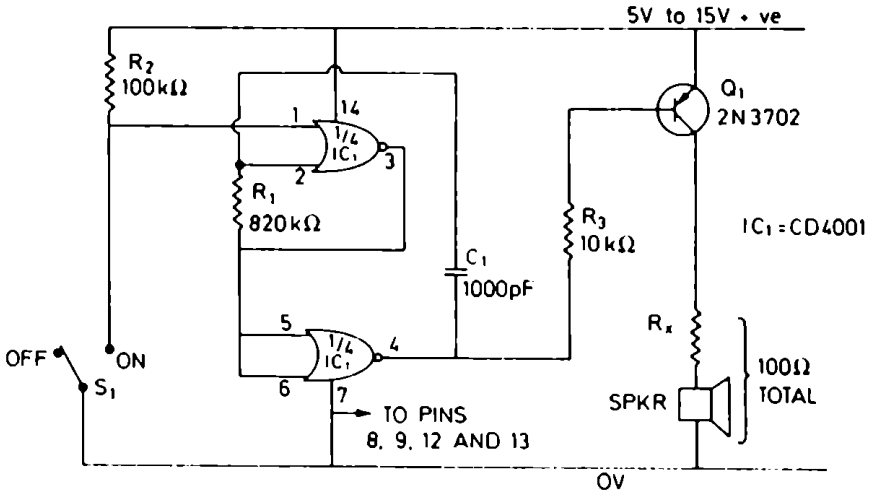


Figure 6.6 Low-power 800 Hz alarm generator

example, shows how the device can be connected for use in a low-power fixed-frequency (monotone) alarm-call generator circuit. Here,

two of the IC gates are interconnected as a gated astable multivibrator that operates at approximately 800 Hz, and the output of the astable is coupled to switching transistor Q_1 via R_3. Q_1 uses the speaker and limiting resistor R_X as its collector load.

The action of the circuit is such that Q_1 is driven alternately on and off at a frequency of 800 Hz when S_1 is closed, so drive current is pulsed into the speaker under this condition. The speaker and limiting resistor R_X should have a total series resistance of about 100 Ω. The available acoustic output power of the circuit depends on the value of supply rail voltage used, and on the impedance of the speaker. Using a 9V supply, the mean output current is fixed at about 40 mA, so that the output power to a 15 Ω speaker is about 25 mW, and to a 100 Ω speaker about 160 mW.

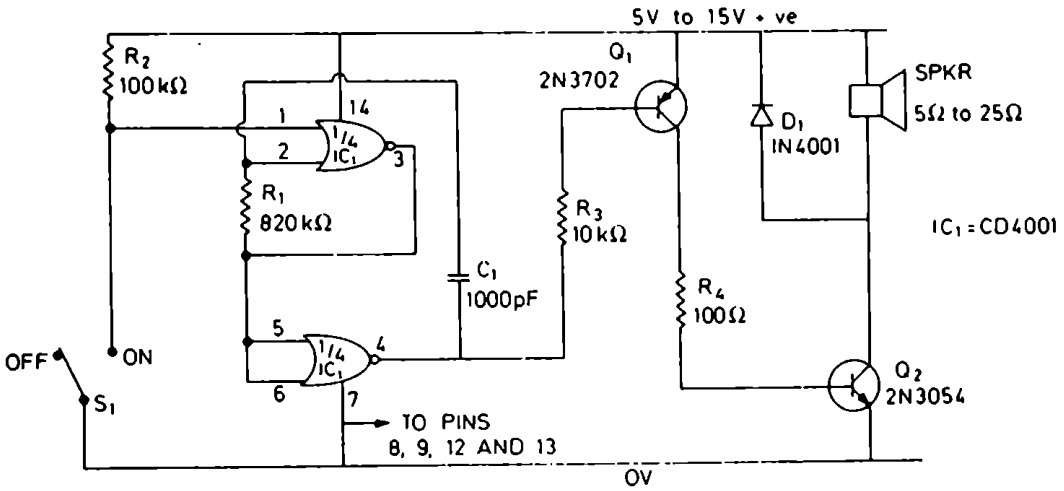


Figure 6.7 Medium-power (0.25 W to 11.25 W) alarm generator

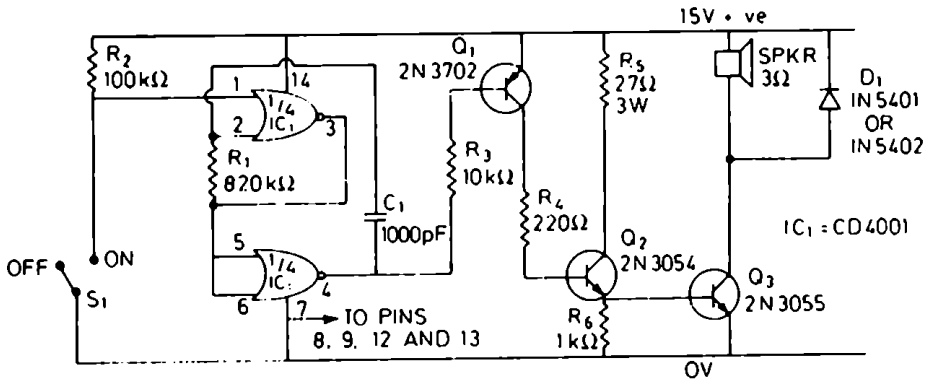


Figure 6.8 High-power (18 W) alarm generator

The output power of the circuit can be boosted to a higher level by modifying the design as shown in *Figure 6.7*. Here, the output of Q_1 is used to provide base current drive to output power transistor Q_2,

which uses the speaker as its collected load. The speaker can have any impedance in the range 5 Ω to 25 Ω, and the supply can have any voltage in the range 5 V to 15 V. The actual output power of the circuit depends on the combination of supply voltage and speaker impedance that is used, and ranges from 250 mW when a 25 Ω speaker is used with a 5 V supply, to 11.25 W when a 5 Ω speaker is used with a 15 V supply.

The output power can be boosted to about 18 W by further modifying the circuit as shown in *Figure 6.8*. Here, transistors Q_2 and Q_3 are super-alpha connected to give high gain, and the circuit is designed to operate from a fixed 15 V supply and to use a 3 Ω speaker.

Note that protection diodes are wired across the speakers in the *Figures 6.7* and *6.8* circuits. These diodes are used to prevent the collector voltages of the output transistors from swinging above the supply-rail voltage as the inductive speaker loads are pulsed with current. The diodes must have current ratings of at least 1 A in the *Figure 6.7* circuit, and at least 3 A in the *Figure 6.8* circuit. Also note that the *Figure 6.7* circuit passes a typical standby current of about 10 μA, and the *Figure 6.8* passes a standby current of about 30 μA, due to the leakage currents of the transistors used.

The three alarm-generator circuits that we have looked at so far each produce a fixed or monotone output which is, by definition, monotonous to listen to. A more attractive and attention-catching sound is made by the basic pulsed-tone low-power alarm generator circuit of *Figure 6.9*

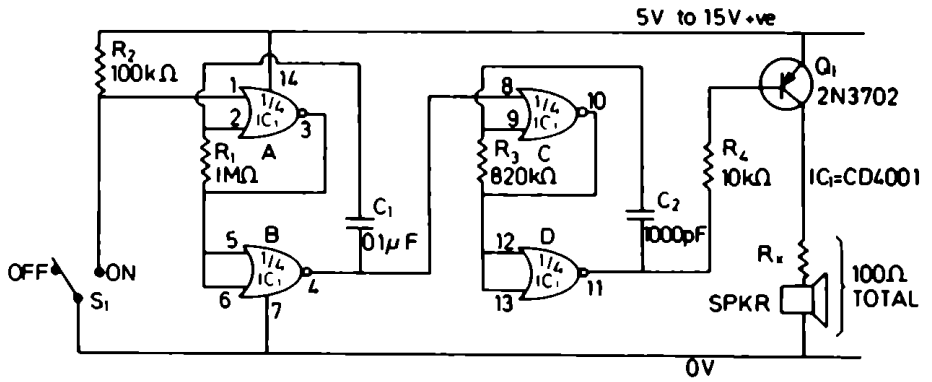


Figure 6.9 Pulsed-tone alarm generator

Here, gates A and B are wired as a fixed-frequency astable multivibrator that operates at a frequency of about 6 Hz and is gated on via S_1, and gates C and D are wired as a fixed-frequency astable multivibrator that operates at about 800 Hz and is gated on and off by the output of the A–B astable. The output of the 800 Hz astable feeds to the speaker via R_4–Q_1 and R_X. Thus, when S_1 is closed, the tone

generated at the speaker comprises an 800 Hz note that is pulsed on and off at a rate of 5 Hz.

Note that the four basic alarm-generator circuits of *Figures 6.6* to *6.9* are shown as being gated on and off via switch S_1. If required, these circuits can be activated by an external voltage by removing S_1 and applying the trigger voltage to pin 1 of the IC. This voltage should vary between OV and the full positive supply rail potential. The alarms are off when this trigger voltage is high, and are on when the trigger voltage is low. As a safety precaution, a 10 kΩ resistor should be wired in series with the pin 1 connection of the IC when using this voltage triggering.

Alternatively, the alarms can be modified so that they are active whenever the power supply is connected, by simply eliminating S_1 and R_2 and shorting pins 1 and 2 of the IC together. In this case the alarms can be turned on and off via a switch or pair of relay contacts wired in series with the positive supply line.

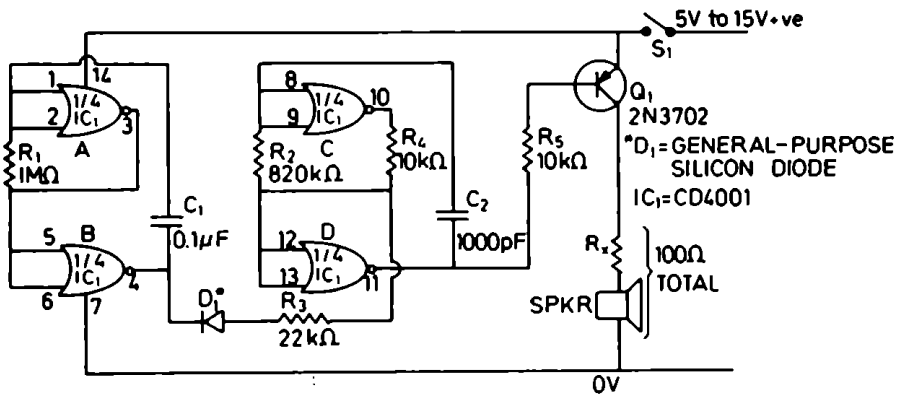


Figure 6.10 Warble-tone alarm generator

The *Figure 6.9* circuit generates a very distinctive 'pulsed' tone. A different but equally distinctive sound can be created by a warble-tone generator. *Figures 6.10* and *6.11* show two warble-tone circuits which develop sound outputs that switch alternately between 600 Hz and 450 Hz at a rate of about 6 Hz. Both circuits operate in the same basic way, as follows.

Gates A and B of the IC are connected as a simple 6 Hz astable multivibrator, and gates C and D are connected as a modified astable that operates at a frequency of a few hundred hertz and has its output taken to the speaker via $R_5 - Q_1$ and R_X. The output of the 6 Hz astable is coupled into the C–D astable via $D_1 - R_3$ and R_4 in such a way that it influences the shape and frequency of the C–D astable waveforms. When the output of the 6 Hz oscillator is high the C–D astable operates at a frequency of approximately 450 Hz, and when the

output of the 6 Hz oscillator is low the C–D astable operates at a frequency of approximately 600 Hz. Thus, a warble-tone sound is generated in the speaker when the circuit is operating.

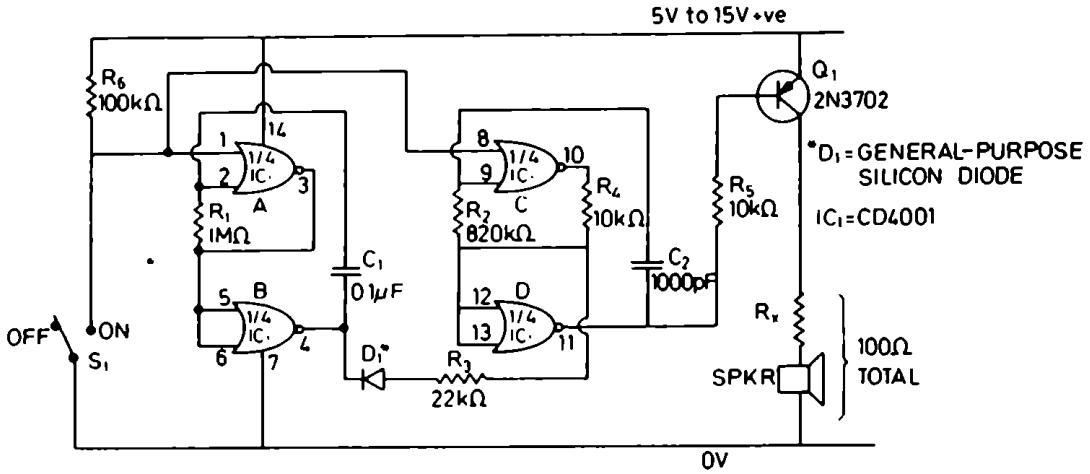


Figure 6.11 Modified warble-tone alarm generator

The two circuits of *Figures 6.10* and *6.11* operate in the same basic way, but differ in their methods of activation. The *Figure 6.10* circuit is designed to be active whenever it is connected to its power supplies so that the alarm can be turned on and off via a switch or pair of relay contacts in series with its supply lines, as shown by S_1. The *Figure 6.11* circuit is intended to be permanently connected to a power supply, and can be activated by low-current switch S_1 or via a variable voltage applied to the low end of R_6.

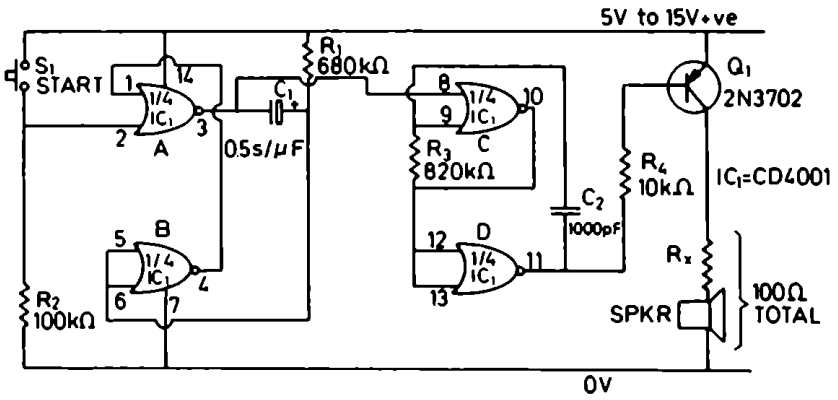


Figure 6.12 One-shot alarm generator

All of the alarm-generator circuits that we have looked at so far are turned on and off manually via a single switch. To conclude this section of the chapter, we show a single one-shot alarm generator, which turns off automatically some pre-set time after it is initially activated, and

two self-latching alarm generators, which automatically lock into the ON state once they are initially activated.

Figure 6.12 shows the circuit of the one-shot alarm generator, which starts to generate a monotone alarm signal as soon as push-button switch S_1 is momentarily closed, but stops generating automatically after a pre-set period. The period can be varied from a fraction of a second to several minutes by selecting the C_1 value.

The operation of the circuit is quite simple. Gates A and B are wired as a gated monostable or one-shot multivibrator which is triggered by momentarily closing S_1, and gates C and D are wired as a gated astable multivibrator that operates at 800 Hz. The output of the monostable is used to turn the astable circuit on and off, and the output of the astable is fed to the speaker via Q_1. Thus, the alarm is normally off, but turns on as soon as S_1 is closed, and then turns off again automatically after a pre-set period. The period is roughly equal to 0.5 s/μF of C_1 value: C_1 must have a leakage resistance of less than 1 MΩ or so.

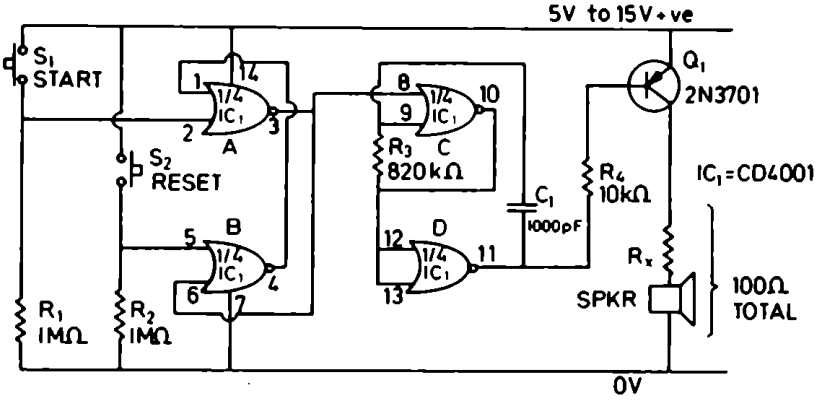


Figure 6.13 Self-latching alarm generator

Figure 6.13 shows the circuit of a self-latching alarm generator, which locks into the ON state and generates a monotone alarm signal as soon as push-button switch S_1 is briefly closed. Once activated, the circuit can be turned off again only by operating RESET switch S_2.

Here, gates A and B of the circuit are wired as a manually-triggered bistable multivibrator, and gates C and D are wired as a gated astable multivibrator. The output of the bistable is used to turn the astable on and off, and the output of the astable is fed to the speaker via R_4–Q_1 and R_X. The action of the circuit is such that the alarm turns on and self-latches as soon as S_1 is briefly operated. The alarm then remains on until S_2 is briefly operated, at which point the alarm resets back into the OFF state, and the quiescent current falls to a microamp or so.

Finally, *Figure 6.14* shows how the above circuit can be modified for use as a break-to-operate self-latching alarm, which turns on and

self-latches as soon as a normally-closed input switch or wire is opened or broken. The two circuits are identical except for the configurations of R_1 and S_1. The *Figure 6.14* circuit can be used as the basis of an excellent burglar-alarm system, as will be shown in the next section of the chapter, and draws a typical standby current of only one or two microamps.

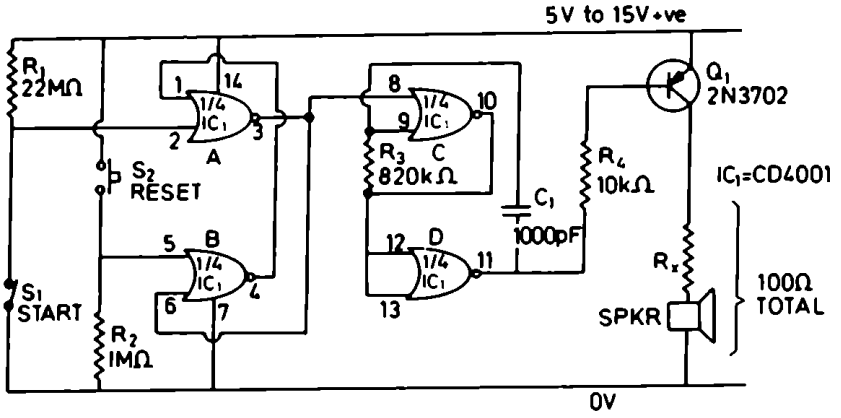


Figure 6.14 Break-to-operate self-latching alarm generator

Note that the circuits of *Figures 6.9* to *6.14* are designed to give only a low output power level, as in the case of the *Figure 6.6* circuit. These circuits can be modified to give medium to high output powers by altering their output stages to conform to *Figure 6.7* or *Figure 6.8*.

Burglar-alarm circuits

A burglar alarm is the most valuable piece of equipment that an electronics enthusiast can build for use in the home. It helps give its owner peace of mind when the house is empty, and gives a high degree of protection against theft of property or damage of premises. It may even help protect the owner's life.

The requirements of the 'ideal' burglar alarm system are stringent. The system must be immune to giving false alarms. It must be battery powered, and consume negligible standby current. It must be capable of driving almost any type of alarm generator (electronic, bell, siren, etc). Finally, the system must be versatile enough to meet the differing needs of individual owners. It should, for example, be capable of providing either self-latch or auto-turn-off operation, and have provision for incorporating 'panic' and other facilities.

In the present section of this chapter we show how you can use the CD4001 COS/MOS IC, in conjunction with a relay and a transistor, to

build your own tailor-made burglar alarms that meet all of the requirements outlined above. Your final alarm system can be as simple or as complex as you want to make it.

The most reliable type of burglar-alarm system is that which is activated by mechanical 'contacts'. These contacts may be normally-open (NO) switches or reed-relays which activate the alarm when they are momentarily closed, or they may be normally-closed (NC) switches or lengths of wire or foil which activate the alarm when they are momentarily opened or broken.

A practical alarm system may be of either the self-latching type, which turns on as soon as it is activated and then remains on indefinitely, or it may be of the auto-turn-off or one-shot type, which turns on as soon as it is activated but then turns off again automatically after a pre-set period. Simple COS/MOS alarm systems of both these types are shown in *Figures 6.15* and *6.16*. Both these circuits have relay outputs, and the relay contacts can be used to activate any type of alarm-generator device.

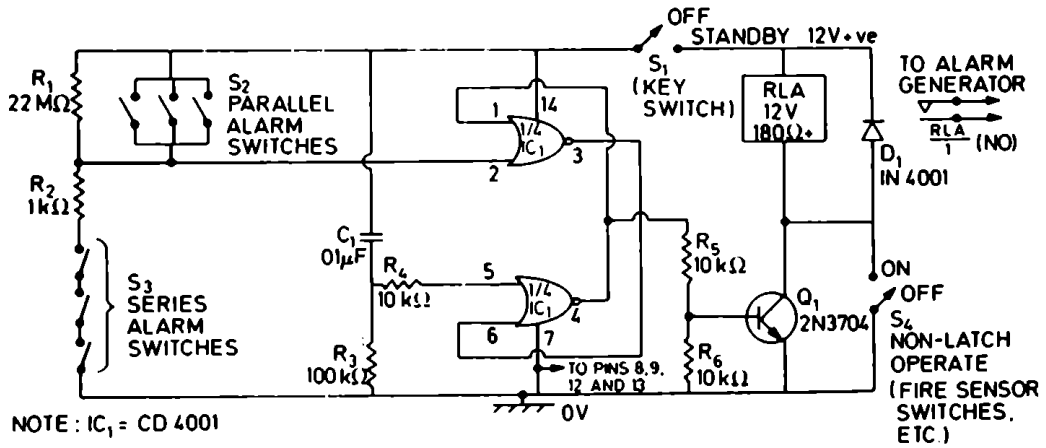


Figure 6.15 Simple self-latching burglar alarm

The self-latching operation of the *Figure 6.15* circuit is obtained by wiring two of the gates of a CD4001 IC as a simple bistable multivibrator. The action of the bistable is such that its output (taken from pin 4) goes low and self-latches when a positive voltage or pulse is applied to pin 5, and its output goes high and self-latches when a positive voltage or pulse is applied to pin 2. Power is applied to the bistable and to the alarm sensor 'contact' switches (S_2 and S_3) via key-operated switch S_1.

Assume, then, that alarm sensor S_2 is open and S_3 is closed. When key switch S_1 is first set to the 'standby' position, pin 2 is held low by the potential divider action of R_1 and R_2, and a brief positive voltage

pulse is fed to pin 5 from the supply line via C_1 and R_3–R_4. Consequently, the output of the bistable automatically goes low as soon as S_1 is closed. Under this condition zero base drive is applied to Q_1, so that Q_1 and the relay and the alarm are all off. The circuit draws a typical current of about 1 μA in this standby mode. Half of this current flows through the supply lines via R_1 and R_2, and the other half flows via the leakage resistance of transistor Q_1.

The alarm can be activated by opening any one of series-connected sensor switches S_3, or by closing any one of parallel-connected sensor switches S_2. Under this condition pin 2 of the bistable goes close to the positive rail voltage, and the bistable changes mode and its output locks into the high state and switches the alarm generator on via Q_1 and the relay. The alarm then stays on indefinitely, and can be turned off only by opening key switch S_1.

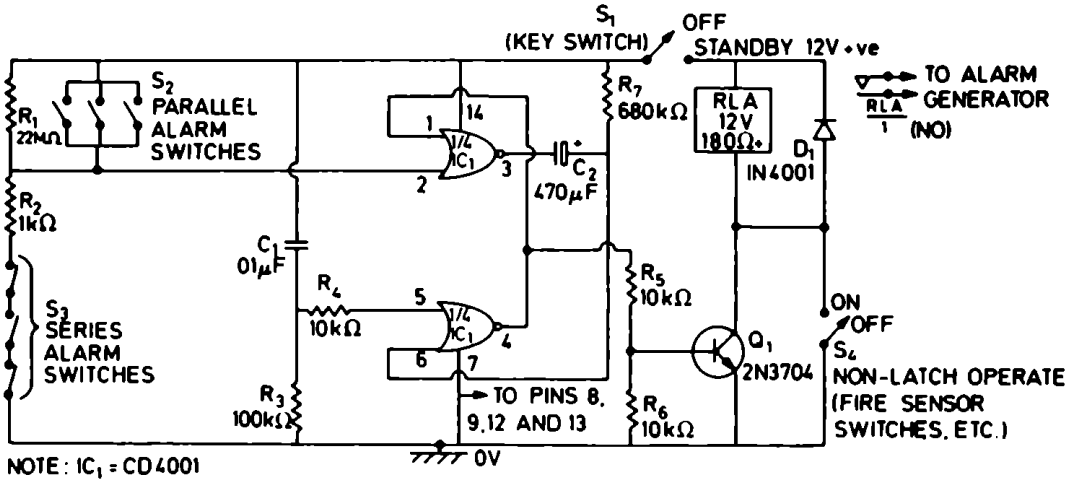


Figure 6.16 Simple auto-turn-off burglar alarm (Turn-off delay ≈ 4 minutes)

The auto-turn-off circuit of *Figure 6.16* is similar to that of *Figure 6.15*, except that in this case the two gates of the IC are connected as a simple monostable multivibrator. The action of this monostable is such that its output goes to the low state when a positive voltage or pulse is applied to pin 5, but goes high for a pre-set period when a positive-going voltage transition is applied to pin 2. The value of this pre-set period is determined by the time constant of R_7 and C_2, and equals approximately 4 min (0.5 s/μF of C_2 value) with the C_2 value shown. At the end of this period the output of the monostable automatically switches back to the low state. Note that the monostable can be triggered only by a positive-going transition of its pin 2 voltage, and its action is not influenced by 'standing' high or low voltages that may be applied to this pin.

Thus, the output of the monostable automatically goes low as soon as key switch S_1 is set to the 'standby' position. Under this condition the relay and the alarm are off, and the circuit consumes a typical standby current of 1 μA.

The alarm can be activated by opening any one of series-connected sensor switches S_3, or by closing any one of parallel-connected sensor switches S_2. Under this condition a positive-going transition appears on pin 2 of the monostable, and its output switches into the high mode for a pre-set period and turns Q_1 –*RLA* and the alarm on. At the end of this period the output of the monostable goes low again, irrespective of the states of S_2 and S_3, and Q_1 –*RLA* and the alarm turn back off. The circuit can then be reset either by opening and then closing S_1, or by setting all S_2 and S_3 switches back to their original conditions.

Note in the circuits of *Figures 6.15* and *6.16* that power is permanently applied to the Q_1 –*RLA* section of the designs, even when S_1 is in the OFF position. This facility enables the alarm to be activated in the non-latching mode at all times via an NO temperature-sensing switch such as a thermostat, so that these circuits can also function as permanently-alert fire-alarm systems. Any number of NO switches can be wired in parallel with S_4.

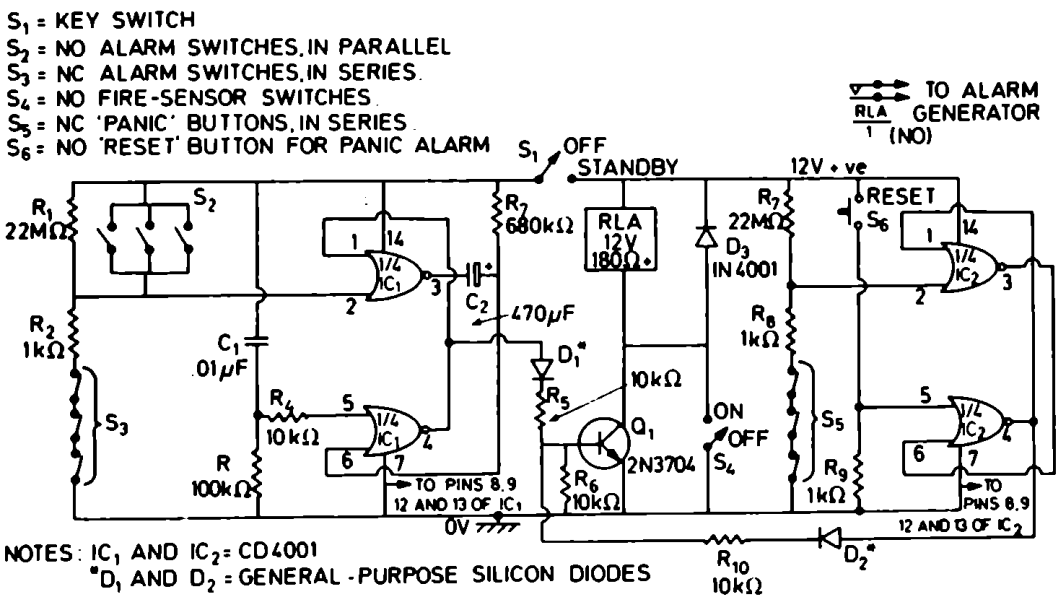


Figure 6.17 Auto-turn-off alarm with 'panic' facility

A weakness of the *Figures 6.15* and *6.16* circuits is that they give no protection against intruders who may break into the house in daylight hours when the main alarm system is switched off. Protection against this type of intrusion can be obtained by scattering a number of

series-connected NC 'panic' buttons around the house, so that a permanently-alert self-latching alarm system can be activated at any time. This facility can readily be added to the *Figures 6.15* and *6.16* circuits, and *Figure 6.17* shows how it can be wired into the auto-turn-off system of *Figure 6.16*.

Here, part of IC_2 is wired as a simple bistable multivibrator circuit that is permanently connected to the supply lines. The output of the bistable is taken to the base of Q_1 via D_2 and R_{10}, so that Q_1 and the relay and alarm can be turned on via the bistable. D_1 is wired in series with R_5 of the main alarm system so that the two sections of the circuit do not interact adversely.

The output of the bistable is normally latched into the low state, so that the relay and alarm are normally off. If any of series-connected panic buttons S_5 are momentarily opened, the bistable immediately changes mode and its output locks into the high state and drives *RLA* and the alarm on. Once the alarm has been turned on, it can be reset to the OFF state by briefly closing RESET switch S_6. This panic facility adds approximately 0.5 μA to the total quiescent current consumption of the complete alarm system.

This panic facility can be added to the *Figure 6.15* circuit by simply wiring D_1 in series with R_5, and adding IC_2 and its associated circuitry to the basic design.

Note in the *Figure 6.17* circuit that two independent CD4001 ICs are used. This is because all four of the gates of each CD4001 IC are connected to the same supply line points (pins 7 and 14), and in the *Figure 6.17* circuit we need to be able to remove the supply from one pair of gates while keeping it on the other. Also note that all unused input pins of the ICs are taken to ground.

Other points to note about the *Figures 6.15* to *6.17* circuits are as follows.

(1) The relay used in each circuit can be any 12 V type with a coil resistance of 180 Ω or greater, and with one or more sets of NO contacts.

(2) Timing capacitor C_2 of the *Figures 6.16* and *6.17* circuits must have a reasonably low leakage resistance, otherwise the alarms may fail to turn off at the end of their pre-set periods. The best way to find out if the capacitor is suitable is to simply put it in the circuit and check that it works alright under very warm conditions.

(3) The three circuits can drive any type of alarm generator (bells, sirens, electronic generators, etc.) via NO relay contact *RLA/1*. Note, however, that these alarm generators must be operated from their own

power supplies, otherwise they may interfere with the electronic functioning of the actual alarm systems.

The three circuits of *Figures 6.15* to *6.17* act as excellent burglar-alarm systems in their own rights. Their capabilities can be considerably expanded, however, by adding on a few simple electronic accessories, as shown in the following sub-section.

Alarm system accessories

A problem with all burglar-alarm systems is that of leaving or entering the house via a protected door once the system has been set into the 'standby' mode. A simple way around the problem is to fit a key-operated by-pass switch to the outside of the door, so that the door sensor switch can be temporarily disabled by the authorised key holder.

In this case the procedure for leaving the house is to first open the door and disable its sensor via the key switch, then re-enter the house and set the alarm to 'standby', then leave the house again, close the door and re-enable its sensor via the key switch. The procedure for re-entering the house without sounding the alarm is to simply disable the door sensor via the key switch, then enter the house and turn the alarm system off.

Most of the tedium of this procedure can be eliminated by equipping the alarm system with an 'exit delay' facility, which automatically disables the door sensor for a pre-set period after the main alarm system is switched to 'standby'. This facility enables the owner to simply switch the alarm system to 'standby' and then leave the house without sounding the alarm. However it is still necessary for the owner to manually disable the door sensor switch on re-entry, if entry is to be made without sounding the alarm.

If required, even this re-entry procedure can be eliminated by equipping the alarm system with a combined 'exit and entry delay' facility. This facility ensures that the alarm will not sound until a pre-set time after the door sensor is initially activated by the entry action, thus giving the owner time to enter the house and turn off or reset the alarm system before the alarm actually sounds.

Practical 'exit delay' facility and 'exit and entry delay' facility circuits are shown in *Figures 6.18* and *6.19*. These facilities can readily be added to any of the main alarm system circuits shown in *Figures 6.15* to *6.17*.

The 'exit delay' circuit of *Figure 6.18* uses three gates of a CD4001 IC. Door sensor switch S_7 can be of either the NO or NC types, and is connected in such a way that the input to pin 1 of gate A is at positive

rail voltage when the door is closed, and is at ground volts when the door is open. Gate A is wired as a simple NOR gate, which gives a low output when either input is high, and time-delay network C_1–R_3 is

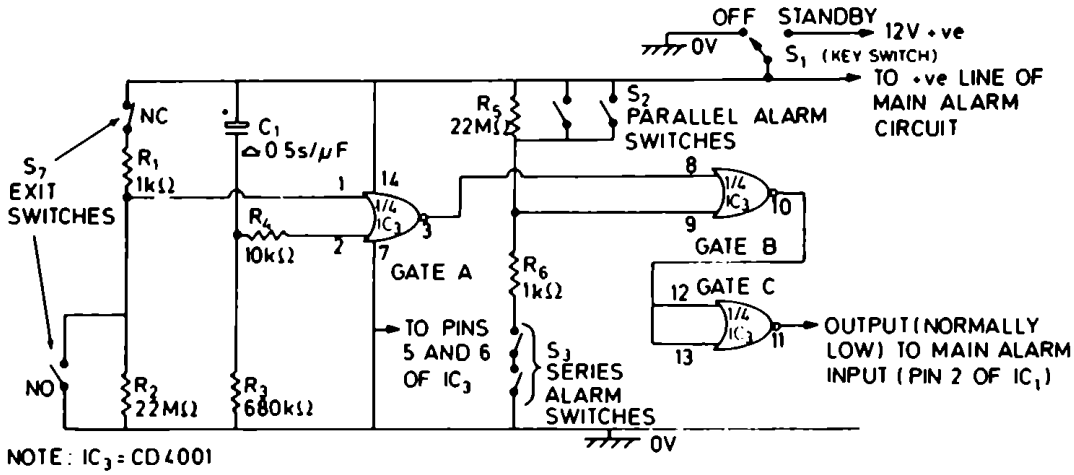


Figure 6.18 Alarm system 'exit delay' facility

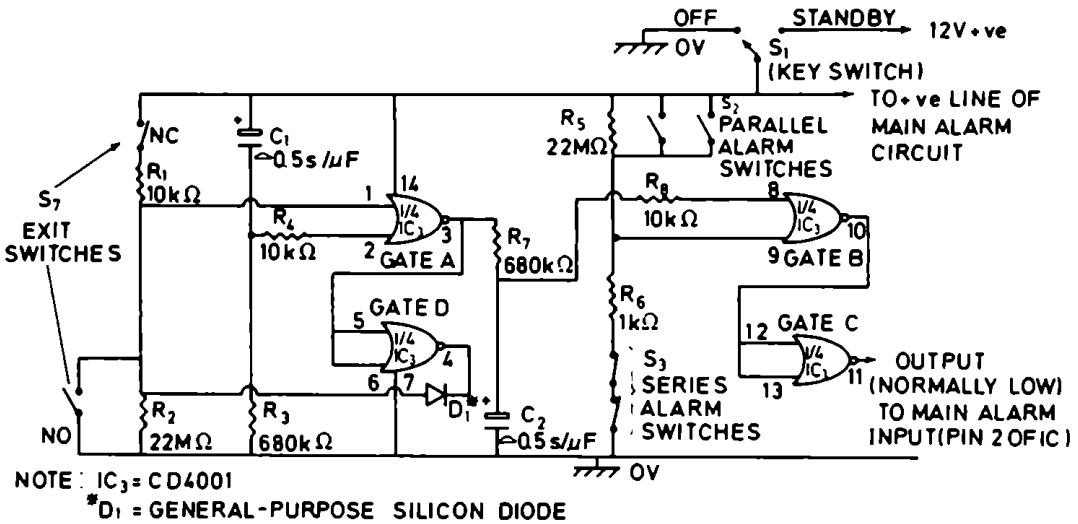


Figure 6.19 Alarm system 'exit and entry delay' facility

connected to the pin 2 input of the gate via R_4. When power is first applied to the circuit, C_1 is fully discharged, so pin 2 is effectively shorted to the positive supply line via R_4, and the output of the gate is at ground volts, irrespective of the state of the door sensor switch.

After a delay determined by C_1 and R_3 (roughly 0.5s/μF of C_1 value) the pin 2 voltage decays to such a value that the gate is influenced by the state of the door sensor switch. If the door is closed at this point the gate output remains low, but if the door is open the output goes high.

The output of gate A is taken directly to pin 8 of gate B, which is also connected as a NOR gate, and the main section of the alarm systems sensor circuitry is taken to pin 9 of this gate in such a way that this pin is effectively grounded under normal conditions. The output of gate B is inverted by gate C, which thus gives an output that is normally low, and this output is passed on directly to pin 2 of IC_1 in the main alarm circuit.

Thus, the action of the *Figure 6.18* circuit is such that all sensor switches except S_7 are enabled as soon as S_1 is set to the 'standby' position, and S_7 is disabled for a pre-set period. At the end of this period S_7 is automatically enabled, and the alarm is able to respond to the actions of S_7.

The combined 'exit and entry delay' facility circuit of *Figure 6.19* is similar to that of *Figure 6.18*, except that R_1 is increased to 10 kΩ, gate A is converted into a self-latching switch with the aid of D_1 and gate D, and the output of gate A is fed to the input of gate B via time-delay network C_2–R_7 and R_8. The action of the circuit is as follows.

When the power is first applied to the circuit all sensor switches are enabled except S_7, which is disabled for a pre-set period via a time-delay network (C_1–R_3). The output of gate A is held in the low state under this condition. At the end of this period S_7 is automatically enabled. If S_7 is activated after the end of this pre-set period, the output of gate A immediately goes high, and is locked in this state by the action of D_1 and gate D. This high output voltage is applied to the input of gate B via time-delay network C_2–R_7, and after a pre-set delay (roughly equal to 0.5 s/μF of C_2 value) the voltage reaching gate B rises to such a value that the alarm is activated.

The 'exit delay' facility or 'exit and entry delay' facility circuits can be added to the main alarm circuits of *Figures 6.15* to *6.17* by simply removing the existing connections to pin 2 of IC_1, by rewiring the existing alarm sensor switches into the *Figure 6.18* or *Figure 6.19* circuits, and by connecting the outputs of the *Figure 6.18* or *Figure 6.19* circuits to pin 2 of IC_1. Note that it is also necessary to wire the OFF pin of key switch S_1 to ground if these facilities are used, so as to provide a discharge path for the timing capacitors of these circuits.

All of the burglar-alarm circuits that we have looked at give reliable performances, and are not prone to giving false alarms under normal circumstances. One 'exceptional' circumstance which may initiate false alarms in any type of alarm system is that of the thunderstorm, when heavy electrical discharges may induce such large energy pulses into the alarm sensor wiring that the alarm is made to trigger falsely. In COS/MOS IC alarm systems this possibility can be eliminated by simply interposing 'sensor transient suppressor' circuits between the outputs of

the main sensor networks and the inputs of the main alarm systems. *Figure 6.20* shows practical circuits of this type.

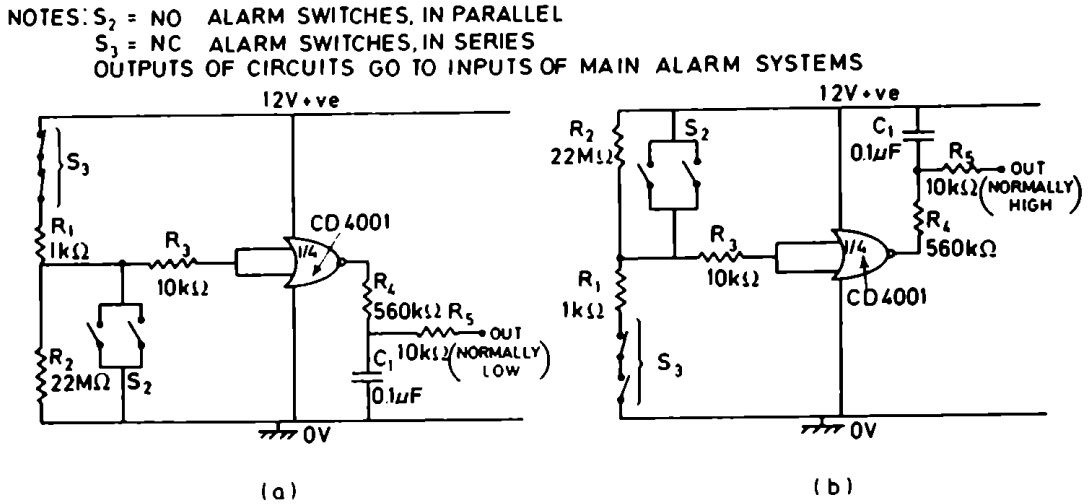


Figure 6.20a Sensor transient suppressor (normally-low output); b Sensor transient suppressor (normally-high output)

In the *Figure 6.20* circuit a spare gate of a CD4001 IC is wired as a basic inverter, and the input of this gate is connected to the output of the main sensor network via limiting resistor R_3. The output of the gate is taken to the input of the main alarm via R_5 and a simple time-constant network formed by C_1–R_4. This network only passes signals that are applied to the gate input for periods greater than 50 mS or so. Consequently, the circuit rejects short-duration spurious pulses that are induced into the sensor wiring, but passes longer-duration signals that are generated by the activation of the sensor switches.

The *Figure 6.20a* circuit is intended for applications where the sensor input to the main alarm system is required to be normally low, and the *Figure 6.20b* circuit is intended for use where the sensor input needs to be normally high. It should be noted that in practice these 'transient suppressor' circuits are only likely to be needed in cases where the lengths of alarm sensor wiring exceed 50 m or so, since all the COS/MOS alarm circuits shown in this chapter have relatively low input impedances (1 kΩ or 10 kΩ) when the sensor switches are in their normal states, and are thus not unduly sensitive to induced signals.

One final accessory that can be added to a burglar-alarm system is an 'intrusion recorder'. This gadget is intended for use in auto-turn-off alarm systems only, and consists of a low-power sound generator that turns on and self-latches if an intrusion occurs, thus giving a continuous indication of the intrusion. The device tells the owner that an intrusion has occurred during his absence from the house, even though the main

alarm has turned off and no signs of the intrusion are visible. A practical 'intrusion recorder' circuit is shown in *Figure 6.21*.

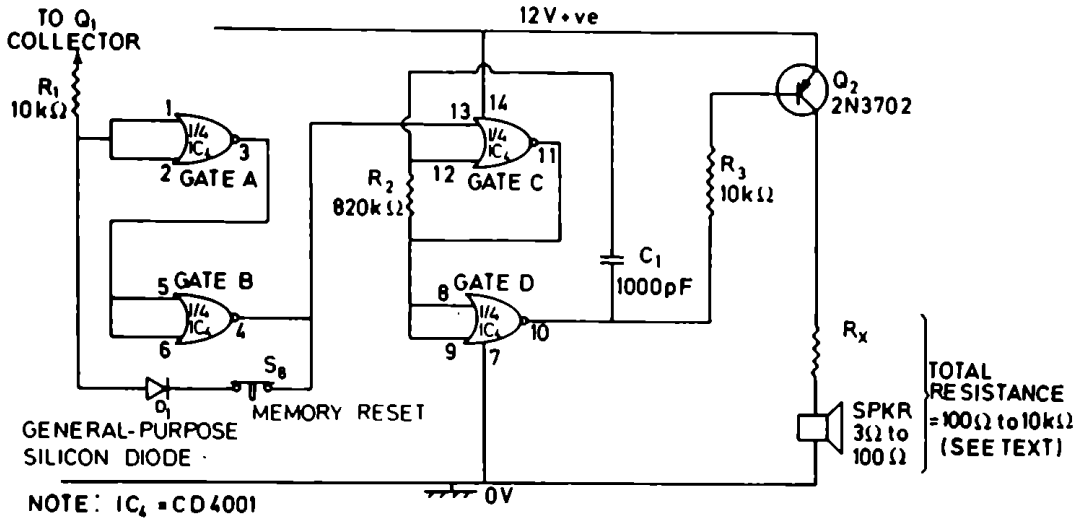


Figure 6.21 Intrusion recorder

The *Figure 6.21* circuit is permanently wired across the supply lines, and its operation is quite simple. Gates C and D are connected as a gated 800 Hz astable, which drives a speaker via Q_2 and R_X, and this astable is activated from the collector of Q_1 of the main alarm system via the self-latching switch formed by gates A and B. Normally, the collector voltage of Q_1 is high and the alarm relay is off, and under this condition the 800 Hz astable is inoperative and the recorder circuit consumes a quiescent current of only 1 μA or so. If the main alarm system is activated the relay turns on for a pre-set period and the collector of Q_1 goes high. Under this condition gates A and B of the recorder turn on and self-latch, and activate the 800 Hz astable, thus causing an audible signal to be generated in the speaker. Once this audible signal has been initiated, it can only be stopped again by operating RESET switch S_8.

The *Figure 6.21* circuit can be added to the auto-turn-off circuit of *Figure 6.16* or *Figure 6.17* by simply wiring it across the supply lines and connecting R_1 to the collector of Q_1. The speaker used in the circuit can have any impedance up to 100 Ω. The combined series value of R_X and the speaker impedance can be varied from a minimum value of 100 Ω up to about 10 kΩ, depending on the sound intensity that is required from the speaker. The maximum power output of the circuit is about 250 mW when R_X has a value of zero and a 100 Ω speaker is used, and in this case the circuit consumes roughly 50 mA of current. Proportionately lower currents are consumed at lower power levels.

S_1 = KEY SWITCH
S_2 = NO ALARM SWITCHES, IN PARALLEL
S_3 = NC ALARM SWITCHES, IN SERIES
S_4 = NO FIRE-SENSOR SWITCHES IN PARALLEL
S_5 = NC 'PANIC' BUTTONS, IN SERIES
S_6 = NO 'RESET' BUTTON FOR PANIC ALARM
S_7 = NO EXIT SWITCH
S_8 = NC MEMORY 'RESET' BUTTON, FOR RECORDER

$D_2 - D_5$ = GENERAL-PURPOSE SILICON DIODES
$IC_1 - IC_4$ = CD 4001

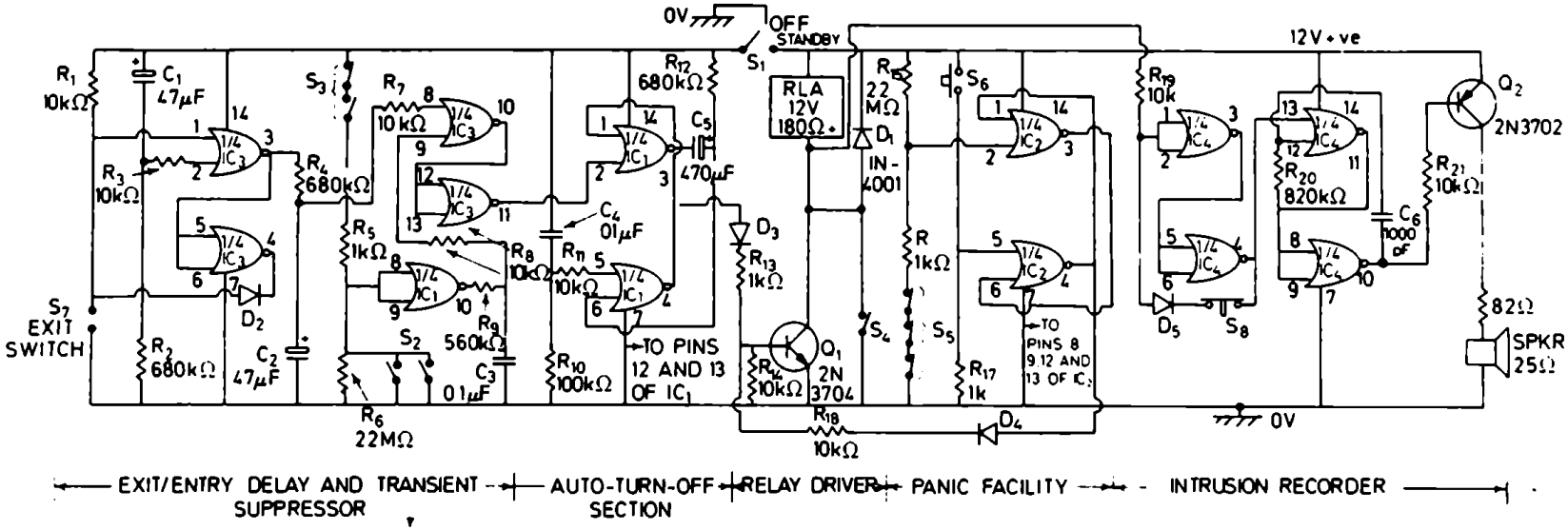


Figure 6.22 Comprehensive alarm system

A comprehensive alarm system

The alarm system accessory circuits of *Figures 6.18* to *6.21* can be added to the basic alarm circuits of *Figures 6.15* to *6.17* in any combination, depending on the requirements of the individual reader. The final alarm system can be as simple or as complex as the reader desires.

The comprehensive alarm system of *Figure 6.22* is shown as an example of how a number of different circuits can be wired together to meet a specific alarm system requirement. In this case the alarm is of the auto-turn-off type, and has a 'panic' facility and an intrusion recorder. The system is intended for use with an NO exit/entry switch, and the system incorporates an 'exit and entry delay' facility, giving delays of approximately 25s in each mode, and has transient suppression applied to the main sensor network. The system has provision for non-latch activation via NO heat-sensing switches, and thus also functions as an automatic fire alarm.

The 'panic' facility is designed around IC_2, and the intrusion recorder is designed around IC_4. Both of these sections of the circuit are permanently wired across the supply lines. The auto-turn-off operation is obtained via IC_1, and one of the spare gates of this IC is used to provide transient suppression for the main sensor network. IC_3 provides the 'exit and entry delay' facility. Finally, note that the OFF terminal of key switch S_1 is taken directly to ground, to provide a discharge path for the system's timing capacitors.

Miscellaneous alarm circuits

To conclude this chapter, *Figures 6.23* to *6.25* show three miscellaneous alarm circuits that are of general interest. One of these circuits can be activated by contact with water or any other reasonably conductive liquid, and the remaining two circuits can be activated by light or by temperature. All three circuits give a low-power pulsed audio output, and make use of a single CD4001 IC.

Figure 6.23 shows the circuit of the pulsed-output water-activated alarm. Here, gates A and B are connected as a gated 6 Hz astable multivibrator, and gates C and D are connected as a gated 800 Hz astable. The 800 Hz multivibrator is gated via the 6 Hz astable, and its output feeds to the speaker via Q_1. The 6 Hz astable is gated via the resistance appearing between a pair of metal probes.

Normally, the two probes are open circuit, and under this condition both astables are disabled and the circuit passes near-zero quiescent current. When a resistance is placed across the probes, a voltage divider

action takes place between this resistance and R_1, and a fraction of the supply voltage is applied to the input terminal of gate A. When this voltage falls below the transition voltage of the IC the two astable circuits become enabled, and a pulsed alarm signal is generated.

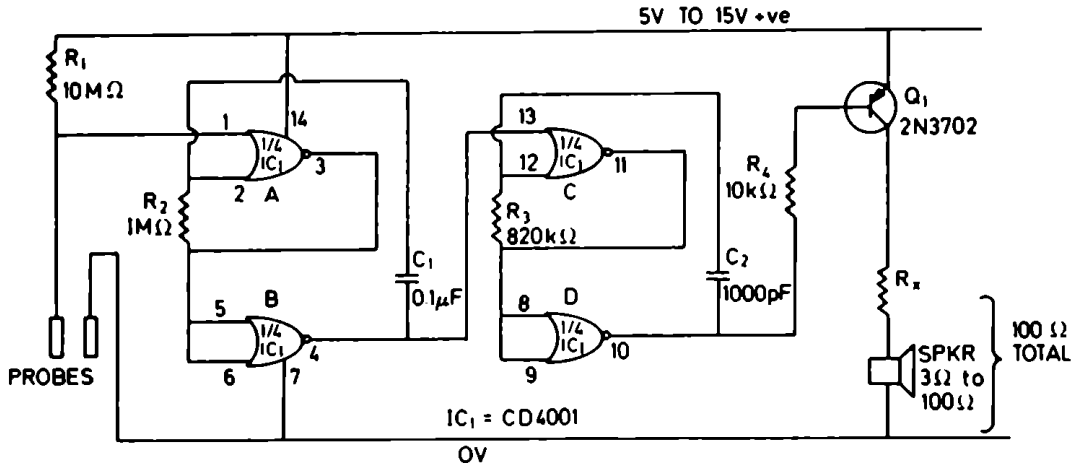


Figure 6.23 Pulsed-output water-activated alarm

COS/MOS ICs have nominal transition voltage values of 50% of the supply voltage. Consequently, the *Figure 6.23* circuit is activated when the probe resistance falls below a nominal value of 10 MΩ. Water, in common with many other liquids, has a fairly low resistance, so that the alarm circuit can be turned on by simply placing both probes simultaneously into water. The circuit thus acts as a water-activated alarm,

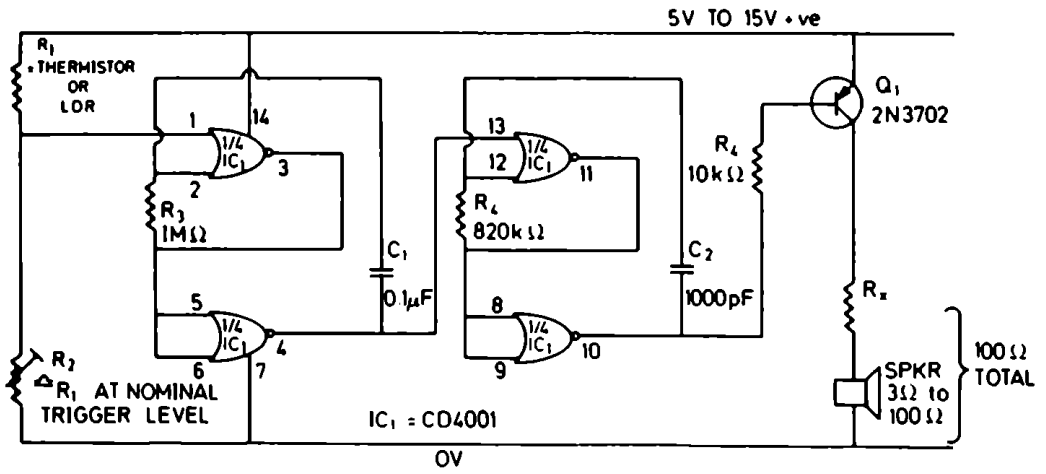


Figure 6.24 Pulsed-output under-temperature or light-activated alarm

and gives a low-level pulsed output. The circuit can be used to indicate flooding in cellars or basements, the overflowing of cisterns or water tanks, or simply to give an announcement when the bath water has reached a pre-determined level.

Finally, *Figures 6.24* and *6.25* show how the above circuit can be modified for use as a pulsed-output temperature or light-activated alarm. In the explanation of circuit operation given above it was

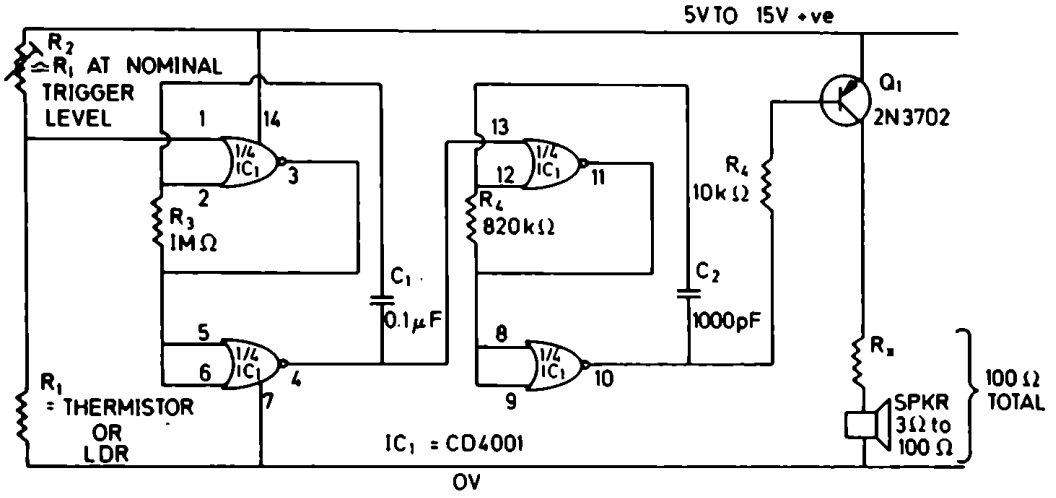


Figure 6.25 Pulsed-output over-temperature or dark-activated alarm

pointed out that the alarm turns on as soon as the input voltage falls below the transition voltage value of the IC. This transition voltage is reasonably stable, and the turn-on action of the alarm is quite sharp. Consequently, the alarm can readily and reliably be activated via a light or temperature-sensitive potential divider wired across the supply lines.

Figure 6.24 shows the connections for making an under-temperature or light-activated alarm, which turns on when the temperature of a thermistor falls below a pre-set level, or when the illumination of a light-dependent resistor rises above a pre-set level. The light or temperature-sensing element(R_1) forms the upper arm of the potential divider, and the sensitivity control R_2 forms the lower arm.

The action of the *Figure 6.24* circuit can be reversed, so that it acts as an over-temperature or dark-activated alarm that turns on when the temperature rises above a pre-set level or when the illumination falls below a pre-set level, by simply transposing the positions of R_1 and R_2, as shown in *Figure 6.25*.

In either case, any negative-temperature-coefficient thermistor can be used as a temperature-sensing element, or any cadmium-sulphide photocell can be used as a light-sensing element. Ideally, however, these elements should have large resistance values at their normal operating levels, so that the quiescent current consumption of the circuits are kept to reasonably low levels. R_2 is a pre-set resistor, and should be adjustable to give a value roughly equal to that of the sensing element at the nominal light or temperature-triggering level. This resistor acts as the circuit's sensitivity control.

15 COUNTING AND DIVIDING CIRCUITS

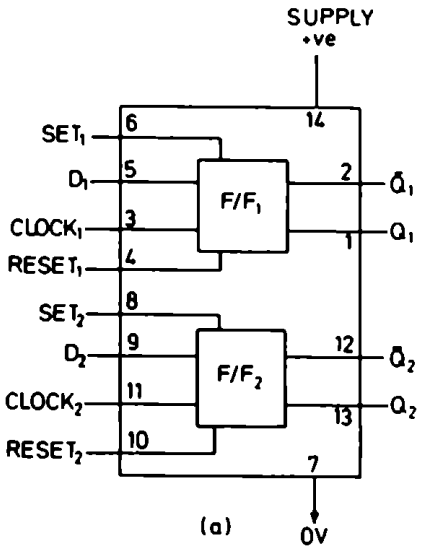
In earlier chapters of this volume we looked at a variety of ways of using simple COS/MOS digital ICs such as the CD4001 and CD4011 quad 2-input NOR and NAND gates. In this concluding chapter of the volume we take a brief look at some simple applications of more sophisticated COS/MOS counting and dividing circuits, to give a further insight into the potential of COS/MOS technology.

The CD4013 dual 'D'-type flip-flop

The simplest counting/dividing IC in the entire RCA COS/MOS line is the CD4013 dual 'D'-type flip-flop. *Figure 7.1a* shows the effective circuit and pin connections of this device, which is housed in a 14-pin dual-in-line package, and *Figure 7.1b* shows the truth table of each of its two 'D'-type flip-flops. The device can be operated from any supply in the range 5 V to 15 V, and can typically operate at clock speeds up to 10 MHz when powered from a 10 V supply.

The CD4013 contains two identical and independent data-type flip-flops. Each flip-flop has independent data, set, reset, and clock inputs, and has both Q and $\overline{Q}$ outputs. By connecting the $\overline{Q}$ output back to the data input, the device can be used for counting and toggle applications. The logic level present at the D input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock, and is accomplished by a high level on the SET or RESET line respectively. The CLOCK pulse of this and all other COS/MOS counting and dividing ICs mentioned in this

chapter must have a rise time of less than 5 μS, and a width greater than 0.5 μS.



CLOCK LEVEL CHANGE	D	R	S	Q	Q̄
↗	0	0	0	0	1
↗	1	0	0	1	0
↘	X	0	0	Q	Q̄
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

NO CHANGE

X = DON'T CARE CASE

(b)

Figure 7.1a Effective circuit and pin connections of the CD4013 dual 'D' type flip-flop; b Truth-table of each half of the CD 4013

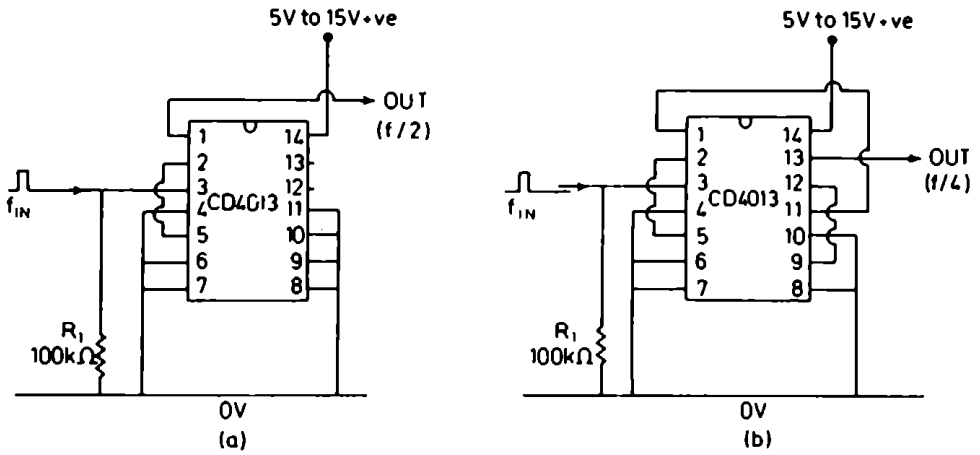


Figure 7.2a Simple CD4013 divide-by-two circuit; b Simple CD4013 divide-by-four circuit

Figure 7.2a shows how one half of a CD4013 can be connected for use as a simple divide-by-two circuit, and *Figure 7.2b* shows how the two halves can be interconnected to act as a divide-by-four circuit. Note in each case that the $\bar{Q}$ output of each used flip-flop is connected back to the D input terminal, that the SET and RESET inputs are grounded, and that the SET, RESET, DATA, and CLOCK terminals of all unused flip-flops are grounded.

Any number of flip-flop stages can be wired in cascade to give any required binary division ratio. Thus, two flip-flops can be wired in

cascade to give a division ratio of 4, or three flip-flops can be used to give a ratio of 8, or four to give a ratio of 16, and so on. Note that the initial clock pulse to the first flip-flop divider stage must have a rise time of less than 5 μS, and should switch fully between the logic 0 and logic 1 levels, and that the change of state of the flip-flop occurs during the positive-going transition of the clock pulse.

If required, a flip-flop can be triggered from non-pulse waveforms, such as sine or ramp signals, by simply feeding these input signals to the input of the flip-flop via a wave-shaping Schmitt trigger circuit, as shown in *Figure 7.3.*

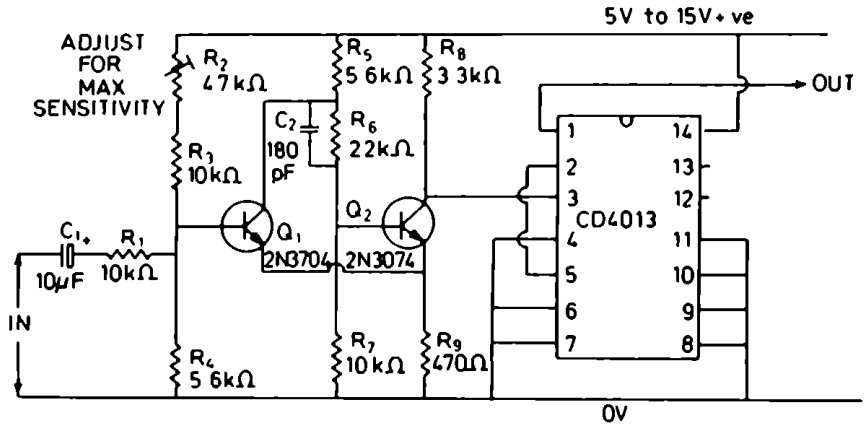


Figure 7.3 Method of triggering a counting/dividing circuit from non-pulse input waveforms.

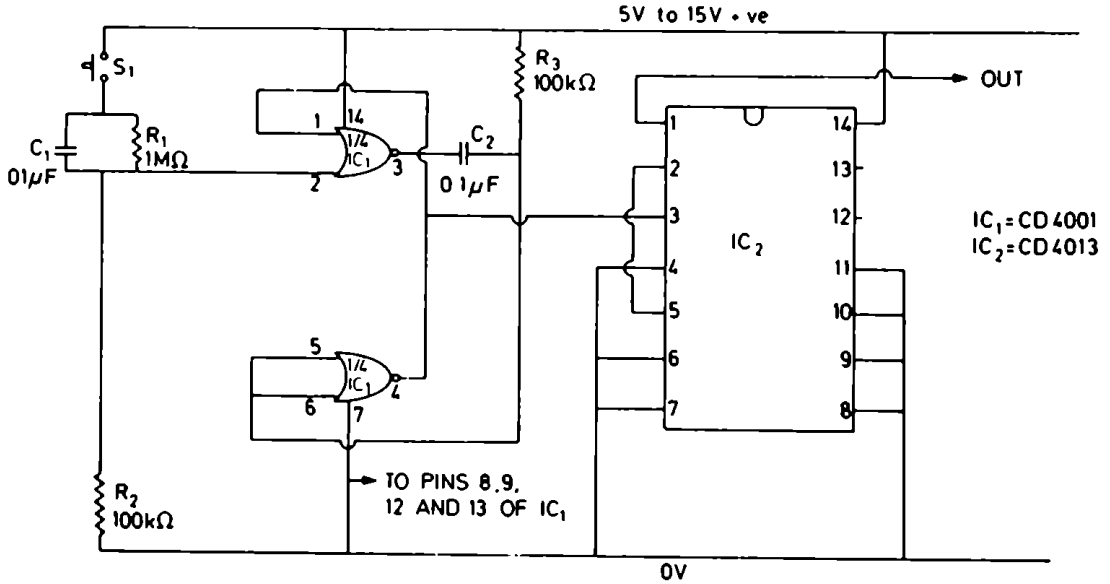


Figure 7.4 Method of manually triggering a counting/dividing circuit

Alternatively, a flip-flop can be triggered via a manually-generated waveform by using the connections shown in *Figure 7.4.* Here, push-button switch S_1 is used to fire a monostable multivibrator, which

generates a fast rise time pulse and thus causes the flip-flop to change state each time that S_1 is operated.

Non-binary division ratios such as 3, 5, 6, 7, 9, and 10, can best be obtained by using a specialised COS/MOS presettable counter/divider IC, such as the CD4018 presettable divide-by-'N' counter, or the CD4017 decade counter/divider.

The CD4018 presettable divide-by-'N' counter

The CD4018 presettable divide-by-'N' counter contains five flip-flop divider stages, plus a considerable amount of logic circuitry. The device can be made to perform a variety of useful functions, including those of dividing by any whole number between 2 and 10. It can be made to divide by 2, 4, 6, 8, or 10 by directly interconnecting selected terminals, and can be made to divide by 3, 5, 7, or 9, by interconnecting selected terminals via one half of a CD4011 NAND gate IC.

The CD4018 is housed in a 16-pin dual-in-line package, and uses the pin notations shown in *Figure 7.5*. The device can be operated from any supply in the range 5 V to 15 V, and can typically operate at clock frequencies up to 5 MHz when powered from a 10 V supply.

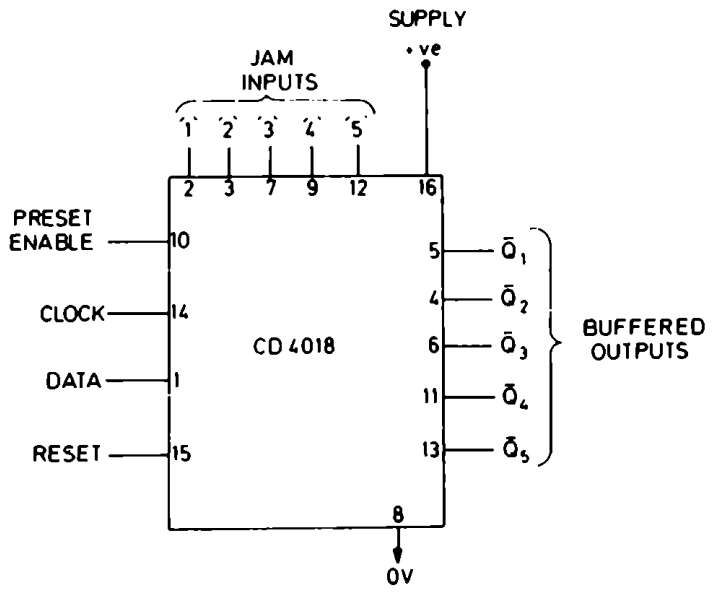


Figure 7.5 Pin notations of the CD4018 presettable divide-by-'N' counter

Figure 7.6 shows how the CD4018 can be connected to divide by 2, 4, 6, 8, or 10, by connecting DATA terminal 1 to $\bar{Q}$ terminals 5, 4, 6, 11, or 13 respectively.

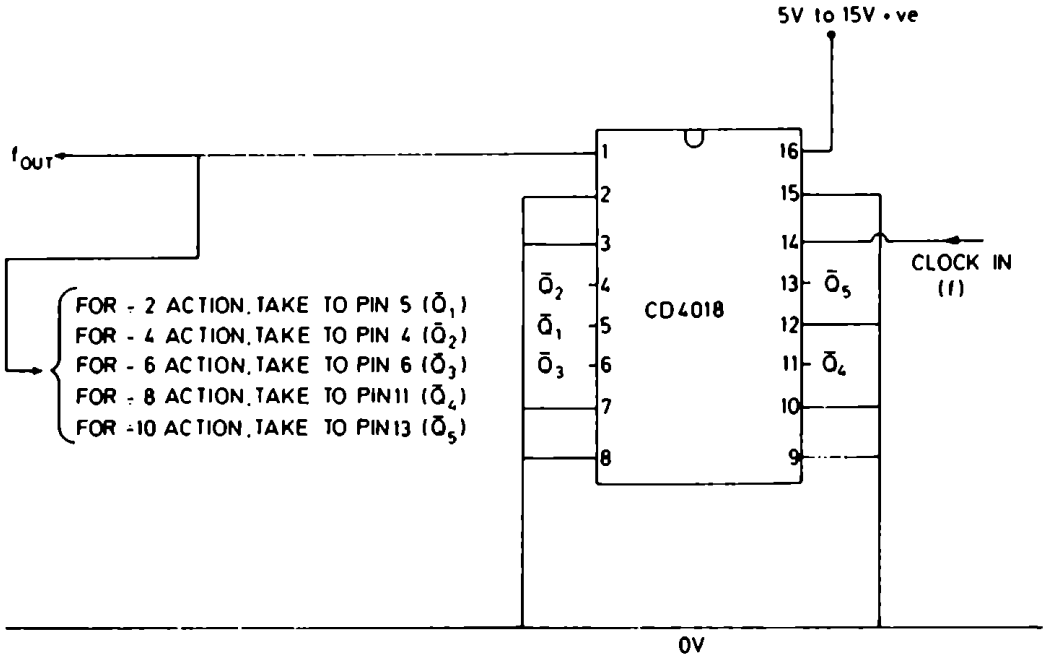
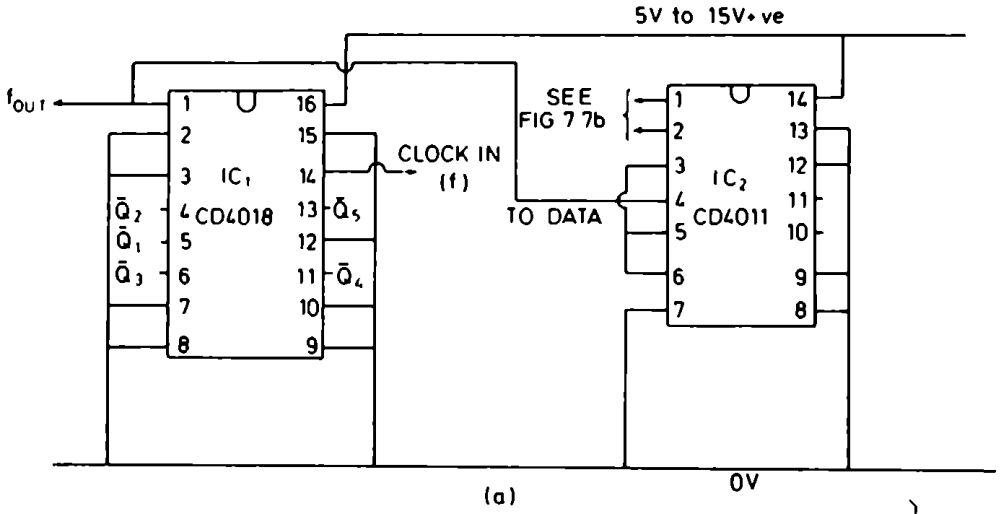


Figure 7.6 Method of connecting the CD4018 for ÷ 2, 4, 6, 8, or 10 operation



FOR ÷ 3 ACTION
- CONNECT PIN 1 OF IC_2 TO PIN 5 ($\bar{Q}_1$) OF IC_1
- CONNECT PIN 2 OF IC_2 TO PIN 4 ($\bar{Q}_2$) OF IC_1

FOR ÷ 5 ACTION
- CONNECT PIN 1 OF IC_2 TO PIN 4 ($\bar{Q}_2$) OF IC_1
- CONNECT PIN 2 OF IC_2 TO PIN 6 ($\bar{Q}_3$) OF IC_1

FOR ÷ 7 ACTION
- CONNECT PIN 1 OF IC_2 TO PIN 6 ($\bar{Q}_3$) OF IC_1
- CONNECT PIN 2 OF IC_2 TO PIN 11 ($\bar{Q}_4$) OF IC_1

FOR ÷ 9 ACTION
- CONNECT PIN 1 OF IC_2 TO PIN 11 ($\bar{Q}_4$) OF IC_1
- CONNECT PIN 2 OF IC_2 TO PIN 13 ($\bar{Q}_5$) OF IC_1

(b)

Figure 7.7 Basic circuit (a) and actual connections (b) for using the CD4018 to give ÷ 3, 5, 7, or 9 operation

Figure 7.7 shows how the CD4018 can be made to divide by 3, 5, 7, or 9, with the aid of one half of a CD4011 quad 2-input NAND gate IC. Thus, divide-by-seven action can be obtained by connecting pin 1 of IC_2 to pin 6 of IC_1, and connecting pin 2 of IC_2 to pin 11 of IC_1.

An alternative COS/MOS IC that can be used for decade or preset-table counting/dividing is the CD4017.

The CD4017 decade counter/divider

The CD4017 decade counter/divider contains five flip-flop dividing stages, plus a considerable amount of logic circuitry. The device is intended primarily for decade counting applications, and gives 10 fully-decoded outputs, plus an overflow or CARRY OUT output. The IC is very versatile, and can be used in a variety of multiplexing applications. When used in conjunction with a single CD4001 quad 2-input NOR gate IC, it can be made to divide by any whole number in the range 2 to 10.

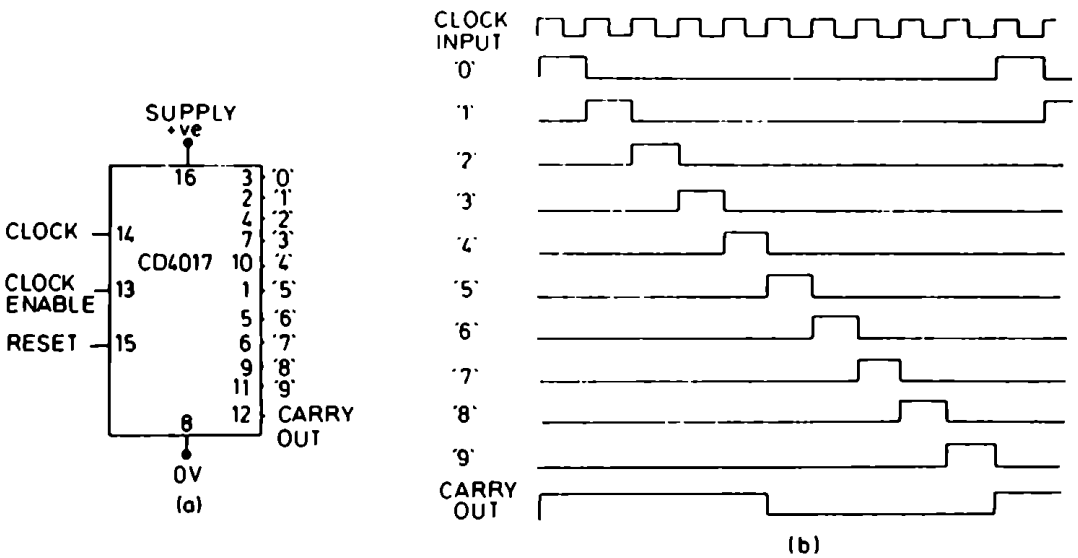


Figure 7.8a Pin notations of the CD4017 decade counter/divider; b Output waveforms of the CD4017, with its RESET and CLOCK ENABLE terminals grounded

The CD4017 is housed in a 16-pin dual-in-line package, and uses the pin notations shown in *Figure 7.8a*. *Figure 7.8b* shows the output waveforms of the device when it is connected as a simple decade divider, with its RESET and CLOCK ENABLE terminals grounded. Note that the output terminals with notations 0 to 9 are normally low or at logic level 0, but sequentially go high or to logic level 1 for one full clock cycle only. The CARRY OUT or overflow signal completes one cycle

for every 10 cycles of input signal. If a fixed-frequency input signal is applied to the IC when it is used in the decade-divider mode, then the CARRY OUT signal is a square wave with a mark/space ratio of precisely 1:1, and a frequency that is one-tenth of that of the input CLOCK signal.

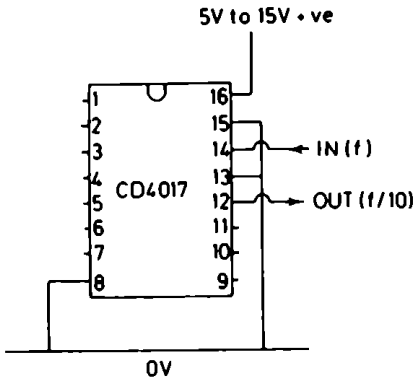


Figure 7.9 Simple CD4017 ÷ 10 circuit

Figure 7.9 shows the practical connections for using the CD4017 as a simple decade divider. If desired, any number of CD4017 divider stages can be connected in cascade to give any desired multi-decade

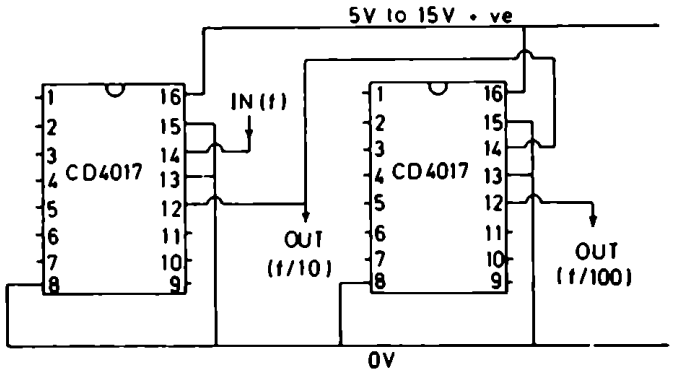


Figure 7.10 Simple CD4017 ÷ 10 and ÷ 100 circuit

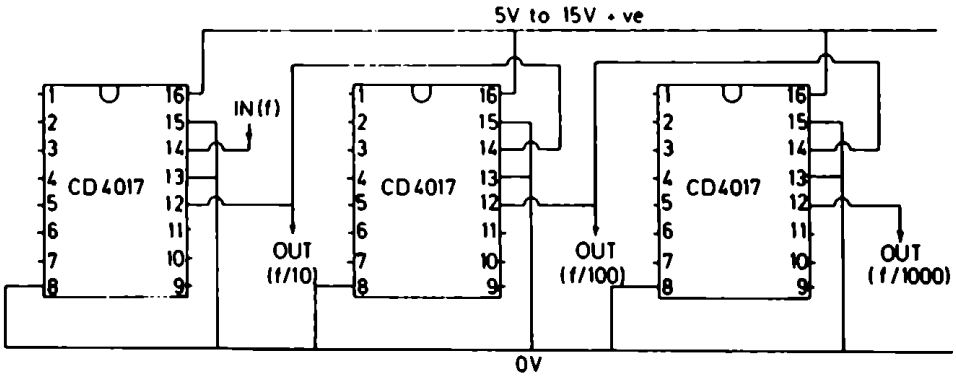


Figure 7.11 Simple CD4017 ÷ 10, ÷ 100, and ÷ 1000 circuit

division ratio. Thus, two stages can be wired in cascade, as shown in *Figure 7.10*, to give an overall division ratio of 100, or three stages

can be wired in cascade, as shown in *Figure 7.11*, to give an overall division ratio of 1000, and so on.

If desired, the CD4017 can be used in conjunction with a CD4001 quad 2-input NOR gate to provide any whole-number division ratio from 2 to 10 by using the connections shown in *Figure 7.12*. Thus, the circuit can be made to divide by three by connecting pin 13 of IC_2 to pin 7 of IC_1, or to divide by seven by connecting pin 13 of IC_2 to pin 6 of IC_1, and so on.

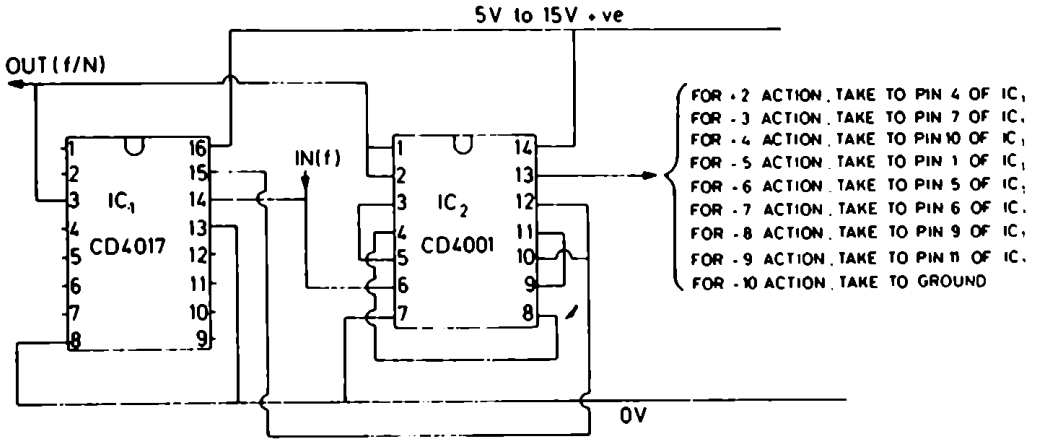


Figure 7.12 Method of using the CD4017 as a divide-by-'N' counter of whole numbers in the range 2 to 10

If decade division is required in conjunction with a visual 7-segment readout, a decade counter/divider with decoded 7-segment display outputs should be used. A suitable COS/MOS IC for this application is the CD4026.

The CD4026 decade counter/divider

The CD4026 decade counter/divider contains five flip-flop dividing stages, plus a considerable amount of logic circuitry. The logic circuitry includes an output decoder, which converts the basic binary code of the IC to a form suitable for directly driving a 7-segment display device, such as an LED display. The device has CLOCK, CLOCK ENABLE, RESET and DISPLAY ENABLE inputs, and seven buffered decoded outputs, plus a decade-divided CARRY OUT output. The device also has DISPLAY ENABLE and UNGATED 'C' SEGMENT outputs.

A useful feature of the device is that the display can be turned on and off via the DISPLAY ENABLE terminal, independently of the actual counting and decoding operation. This feature can result in considerable power saving, since the display need only be activated

when required, and also facilitates the implementation of display multiplexing.

The CD4026 is housed in a 16-pin dual-in-line package, and uses the pin notations shown in *Figure 7.13a. Figure 7.13b* shows the segment designations that must be given to any 7-segment readout device that is used in conjunction with the CD4026.

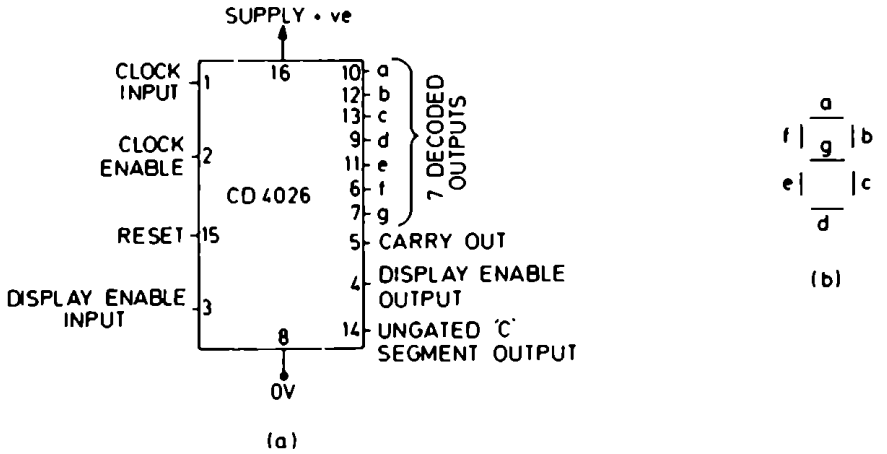


Figure 7.13a Pin notations of the CD4026 decade counter/divider; b 7-segment readout designations to be used in conjunction with the CD4026

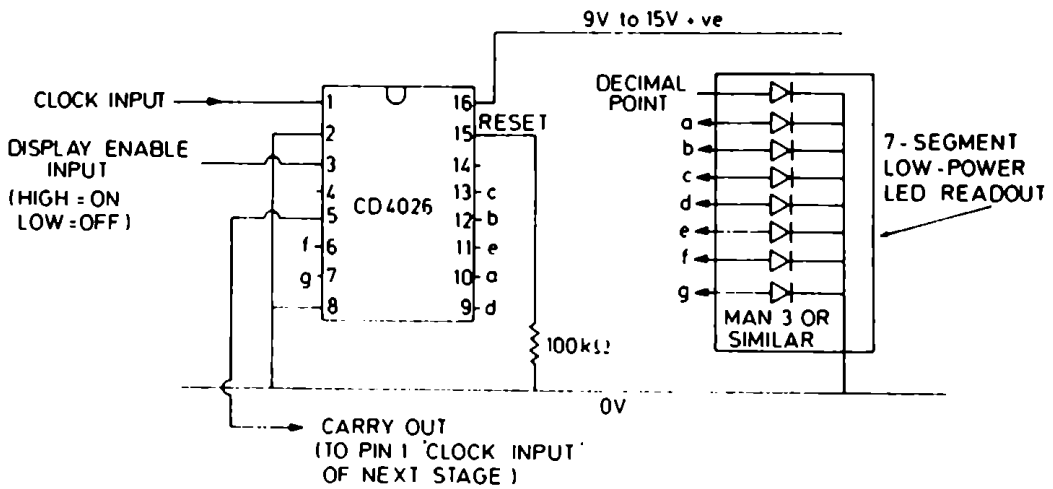


Figure 7.14 Practical CD4026 decade divider/readout unit with low-power 7-segment LED display

The CD4026 can be used in conjunction with a variety of 7-segment display devices, including LEDs, incandescent readouts, neon readouts, and low-voltage vacuum fluorescent readouts. Complete details are given in RCA application note ICAN-6733. For the present, we show only a single typical method of using the CD4026, in conjunction with a low-powered LED display device such as the Mansato MAN 3 or

equivalent. Specific pin numbers of the display device are not shown, but their basic designations are.

The simplified practical circuit of the decade divider/readout unit is shown in *Figure 7.14.* Here, the 'a' to 'g' terminals of the display device are connected to those of the CD4026, and the CLOCK input signal is applied to pin 1 of the CD4026. The pin-3 DISPLAY ENABLE input of the IC should be tied to ground or to the positive rail, either directly or via a 100 kΩ resistor. If the pin is high, the display will be enabled, and if the pin is low the display will be disabled. The pin-15 RESET terminal is normally tied to ground via a 100 kΩ resistor. The counter can be reset to zero by briefly applying a 'high' signal to the RESET terminal.

If several decade divider/display stages are to be wired in cascade, the pin-5 CARRY OUT signal of each CD4026 should be used to provide the pin-1 CLOCK signal of the following CD4026 stage. Any number of stages can be wired in cascade, to give any number of decade display outputs.

Applications of counter/divider circuits

Counter/divider circuits can be used in a variety of applications that are of interest to both the amateur and professional engineer. Several such applications are described in this concluding section of this volume.

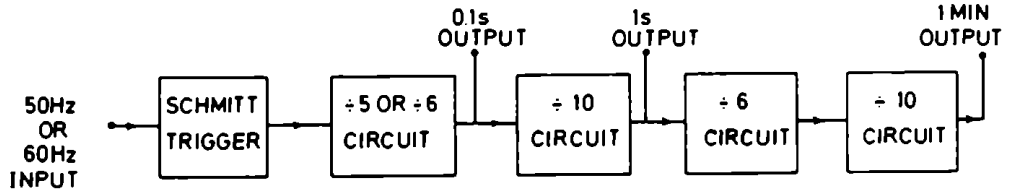


Figure 7.15 Line-synchronised frequency standard

Figure 7.15 shows the block diagram of a line-synchronised frequency standard, which gives accurate output pulses with standard cycling periods of 0.1s, 1s, and 1 min. Here, a standard 50 Hz or 60 Hz signal is tapped off from the a.c. power line, and is then converted to a square wave in a Schmitt trigger; this square wave is then used to drive a divider chain, which in turn gives the accurate output pulses with the cycling periods mentioned above.

The 0.1s output is obtained by dividing by 5 in the case of a 50 Hz input, or by 6 in the case of a 60 Hz input. The 1s pulse is obtained by further dividing by 10, and the 1 min pulse is obtained by further dividing by 6 and 10. One hour output pulses can be obtained by

further dividing by 6 and 10, if required. All of these output pulses have the same degree of accuracy as the power line frequency. In the UK and the USA this accuracy is better than 0.1%.

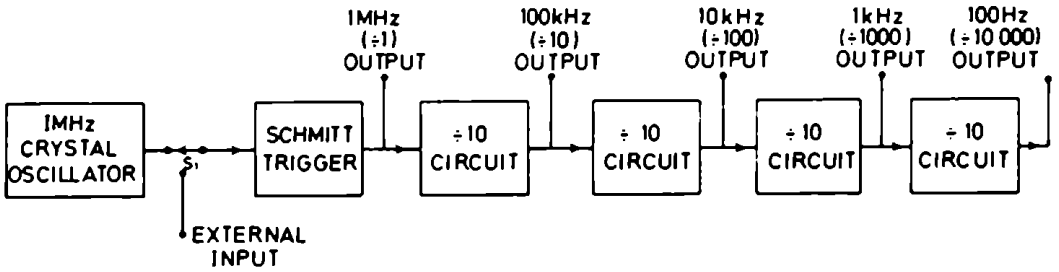


Figure 7.16 Precision frequency standard/frequency divider

Figure 7.16 shows the block diagram of a precision frequency standard/frequency divider. Here, a frequency divider network is made up of a Schmitt trigger and four decade dividers; the input to this network can be taken, via S_1, from either an external source or from an internal 1 MHz crystal oscillator. Consequently, when S_1 is switched to the internal source, the unit generates precise frequency standards of 1 MHz, 100 kHz, 10 kHz, 1 kHz, and 100 Hz. Alternatively, when S_1 is switched to the external source, the unit acts as a precision divider that gives division ratios of 1, 10, 100, 1000, and 10000.

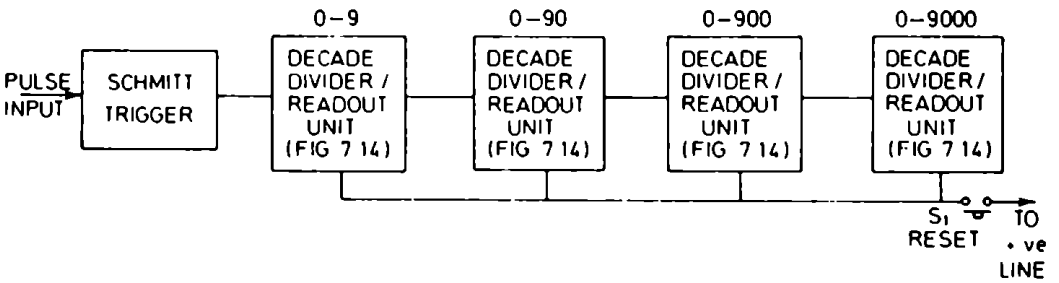


Figure 7.17 High-speed 0-9999 counter, electronic pulse input

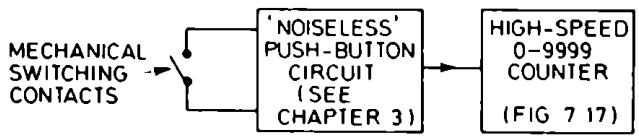


Figure 7.18 High-speed 0-9999 counter, mechanical switch input

Figures 7.17 and *7.18* show the circuits of high-speed 0 to 9999 counters. The *Figure 7.17* circuit can be operated directly from electronic input pulses, such as the output pulses of light-activated electronic switches, etc. The circuit can be operated at very high speeds, and is thus not suitable for operation via mechanical contacts, which are invariably 'noisy'.

If the circuit is to be operated from a mechanically switched input, the input must first be applied to a 'noiseless' push-button multivibrator circuit, to eliminate the effects of contact bounce, as shown in *Figure 7.18*. The ON periods of the multivibrator must be short relative to the periods between operations of the input switch.

It should be noted here that, for the sake of simplicity, the readout units in the above circuits have been shown as reading from left to right. In a practical circuit the readout units should of course be mounted in the reverse order, with the 0 to 9000 indicator on the left and the 0 to 9 indicator on the right.

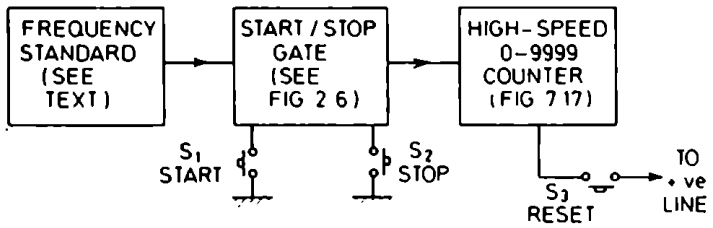


Figure 7.19 Elapsed-time indicator

Figure 7.19 shows the block diagram of an elapsed-time indicator. In use, the counter is first emptied by operating RESET button S_3. The counting operation can then be initiated by operating START button S_1, at which point the START/STOP gate opens and regular input pulses are applied to the counter unit. The timing period is terminated by operating S_2, at which point the gate closes, giving a total elapsed-time readout on the counter.

The frequency used for the frequency standard depends on the time periods that are to be indicated. If a 1 MHz standard is used (giving 1 μS input pulses), the circuit can measure maximum times of only 9999 μS. If a 100 Hz standard is used (giving 10 mS input pulses), the circuit can measure maximum times of 99.99s.

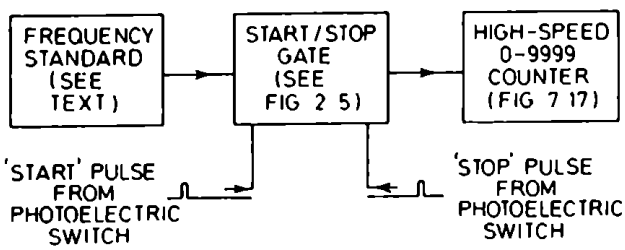
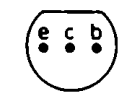


Figure 7.20 Sports-event timer with photoelectric triggering

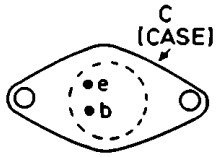
Finally, to conclude this volume, *Figure 7.20* show how the above circuit can be simply modified for use as a sports-event timer, with photoelectric triggering.

APPENDIX
SEMICONDUCTOR OUTLINES AND PIN DESIGNATION

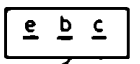
NOTE: In case of difficulty, U.K readers can obtain all semiconductor devices mentioned in this volume from Arrow Electronics Ltd., 7 Coptfold Road, Brentwood, Essex, UK.



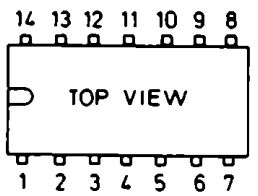
2N3702 AND
2N3704
TRANSISTORS



2N3054 (TO-66 CASE)
AND
2N3055 (TO-3 CASE)
TRANSISTORS

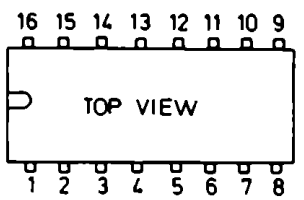


METAL PAD
(COMMON TO COLLECTOR)
MJE 3055
AND
MJE 2955
TRANSISTORS



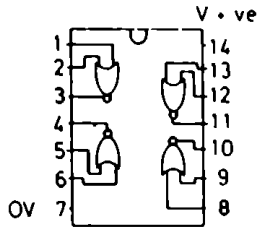
14-PIN d.i.l OUTLINE

[USED ON
CD4001
CD4011
CD4013]

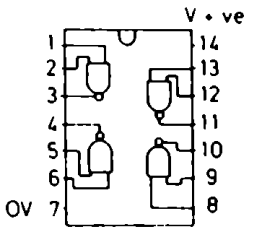


16-PIN d.i.l OUTLINE

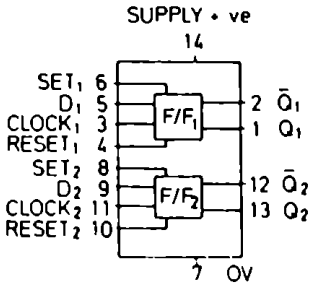
[USED ON
CD4017
CD4018
CD4026]



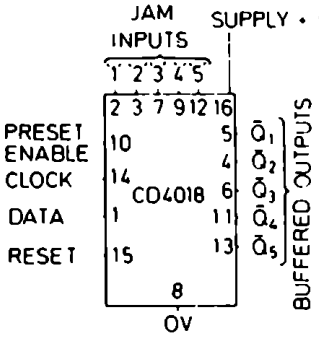
PIN DESIGNATIONS OF THE CD4001 QUAD 2-INPUT NOR GATE



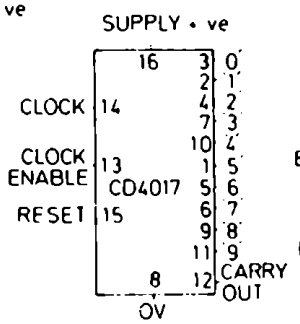
PIN DESIGNATIONS OF THE CD4011 QUAD 2-INPUT NAND GATE



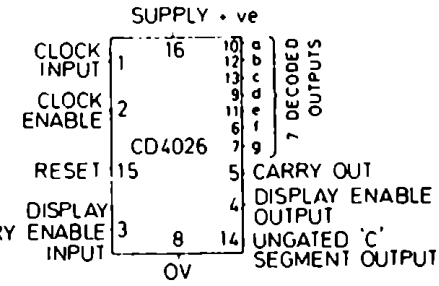
PIN DESIGNATIONS OF THE CD4013 DUAL 'D'-TYPE FLIP-FLOP



PIN DESIGNATIONS OF THE CD4018 DIVIDE-BY-'N' COUNTER

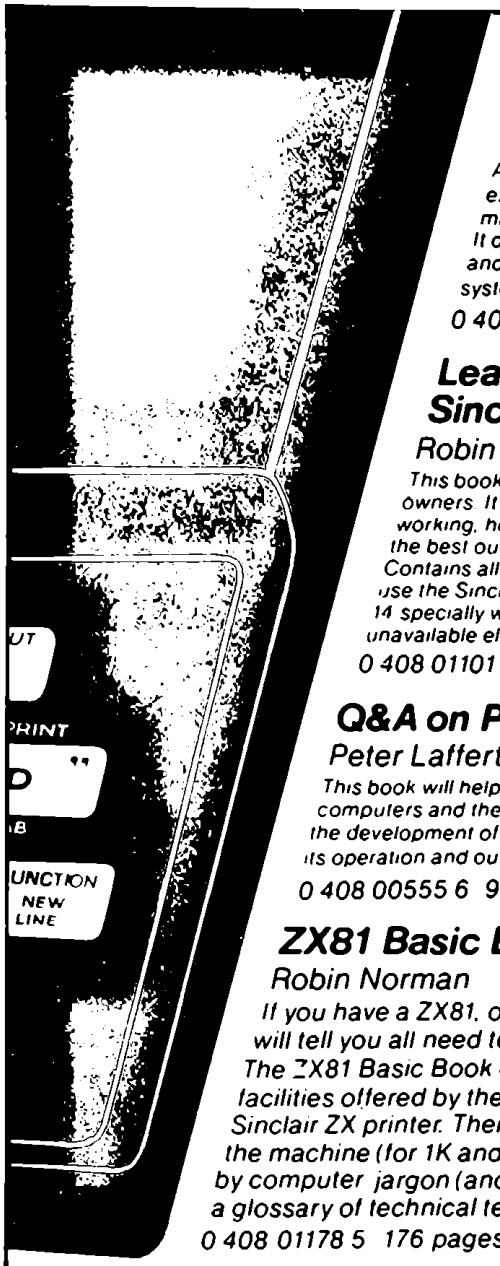


PIN DESIGNATIONS OF THE CD4017 DECADE COUNTER / DIVIDER



PIN DESIGNATIONS OF THE CD4026 DECADE COUNTER / DIVIDER

INDEX



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